Beetle Wafer Selection Criteria

Aldo F. Saavedra
LHCb group
Glasgow University
a.saavedra@physics.gla.ac.uk

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1 Introduction

The chips on a wafer are an unknown quantity when they arrived from the foundry. It is likely, since the wafer has been released, that it has pass all the quality controls imposed on its fabrication. This should guarantee a basic level of functionality of the chip. A step usually referred to *wafer probing* is performed to characterise the performance of all the chips individually before the wafer is diced. Once data is collected from a large sample a selection criteria can be developed.

In this report the selection criteria developed to select the front end chips for the VeLo detector will be presented. The main goal of the development has been to obtain, from the chips available, a batch that is fully functional and uniform on its performance. The variables that were used for selection and the dependency of the yield on limits set on these variables will be presented and described.

2 The Beetle Front End

The VeLo module is double sided with single sided sensors glued back to back. The sensors are instrumented with strips of different pitch and length [1]. The front end chip(FE) employed for the readout of the module is the *Beetle* 1.5 developed by Heidelberg [2]. A complete VeLo detector is composed of 88 modules sensors with each sensor requiring for complete readout of its channel 16 FEs. This mean that the minimum number of FEs needed for the complete production of the VeLo is 1408. The *beetle* chip can operate in binary and analogue mode but only the analogue mode has been configured on the measuring planes of the VeLo. Hence the focus will be in the functionality of the chip that affects this mode of operation.

3 The Wafer Probing

In this section a brief description of the measurements performed during wafer probing is given. The first part is a summary of the measurements and the result that are located in the *adq* files. The second section deals with the different runs that were performed to obtain this data. (By no means this is extensive and covers the complete list of measurements but it does show what was used to develop the selection criteria)

3.1 Measurements Performed

The measurements performed during the wafer probing that are found within the *adq* are summarised in table 3.1. The terms used in the analogue section are illustrated in figure 1. The figure shows the pulse obtained from the test channel together with the variable that are used to describe its performance. The different bias settings used during these measurements are listed in table 2.

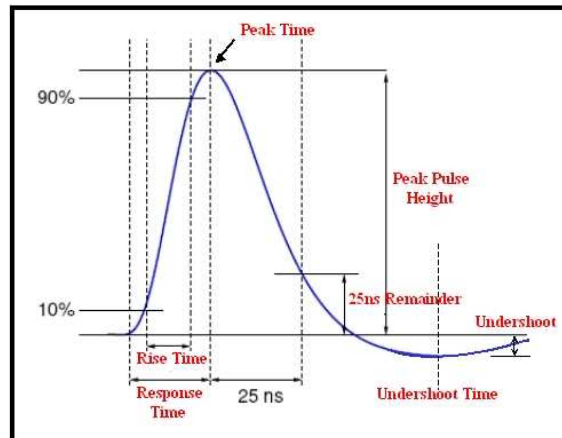

Figure 1: The typical analogue pulse of a readout channel. The variables extracted during the wafer probing are highlighted.

Section	Test	Units	Description
Current	Power On	A	The Chip initialised with S0 settings
	Operational	A	
Headers	Cross Talk	%	Performed on the four ports
	Amplitude Mean	ADC value	
	Amplitude RMS	ADC value	
Analogue	Signal/Noise		Performed under 1 setting
	res pedestal/noise		Channel Histogram
	relative gain		Channel Histogram
	Response Time	ns	Referred to as *t90*, Channel Histogram 4 Settings.
	Rise Time	ns	Referred to as *t90 - t10*, Channel Histogram, 4 Settings.
	Peak Pulse Height	ADC value	Channel Histogram, 4 Settings
	25ns Remainder/Peak Height		Channel Histogram, 4 Settings
	Undershoot-Peak Time	ns	Channel Histogram, 4 Settings
	Undershoot/Peak Height		Channel Histogram, 4 Settings
Registers	IVoltBuf	A	Pipeamp buffer bias current.
	Itp	A	Test pulse bias current.
	Ithmain	A	Current defining common comparator threshold.
	Ithdelta	A	Current defining incremental comparator threshold.
	Isha	A	Shaper bias current.
	Isf	A	Multiplexer bias current.
	Iscurrbuf	A	Output buffer bias current.
	Ipre	A	Preamplifier bias current.
	Ipipe	A	Pipeamp bias current.
	Icomp	A	Comparator bias current.
	Ibuf	A	Front-end buffer bias current.

Table 1: The table present a summary of the measurements performed during the Beetle wafer probing whose result is found in the *adq* for a given chip. The four bias settings are described in table 2 All the registers are 8bits and measurements were performed for 9 dac values (0,1,2,4,8,16,32,127).

Register	Settings			
	0(default)	**1**	**2**	**3**(VeLo)
ITP	22	34	22	24
VFS	0	0	36	56
VFP	0	0	0	20

Table 2: The bias values that were changed for each settings for which the measurements were performed.

3.2 The Wafer Probing Scans

During the wafer probing six different scans are employed to exercise different functionality of the chip[3]. These are:

1. **Digital Test**: Negative test pulse scan with 100% occupancy random trigger.
2. **Pipeline scan**: The pipeline columns are stepped sequentially without test pulse enabled.
3. **Positive Pulse Pipeline Scan**: Positive test pulse with 100% occupancy steped through all pipeline columns sequentially.
4. **Negative Pulse Pipeline Scan**: Negative test pulse with 100% occupancy steped through all pipeline columns sequentially.
5. **Positive Pulse Scan**: Positive test pulse scan with 100% occupancy with random triggers.
6. **Negative Pulse Scan**: Negative test pulse scan with 100% occupancy with random triggers.

The results obtained from these scans provide a extensive characterisation of the chip. A number of parameters were defined to describe the performance of the chip. The quality of the chip was judge by comparing the value for each parameter within a defined range. A variable denoted as *status* was set to the value 0 in the *adq* file if all the parameters were within range. The parameters extracted and their ranges together with the scans performed to obtain their value are described next:

- **Digital Circuitry**- For all scans it was expected that:
  - No empty events.
  - No stuck bits
  - No header bit errors - All parities are OK and no increments in SEU counter.
  - No Pipe Column Number(PCN) errors - All PCNs must be within the range 0-186 and none are lost.
  - For Scans 2,3 and 4 expect all sequential triggers are OK - PCN is incremented by 1 and the distance between the expected and the actual PCN is 0.
- **Header Analysis(All Scans)**
  - Header Cross Talk $<=$ 10% for all ports.
  - All Header Amplitudes are $>=$ 30 ADC counts.
  - The difference between the Maximum and Minimum header $<=$ 20 ADC counts.
  - Significance header amplitude/header RMS $>=$ 20.
- **Front End characteristics:**
  - **Pulse Shape** - Measurements were performed with Scan 5 and 6. The measurements were affected by needle contact although Beetle 1.5 was less susceptible to this because of improved power routing. For all channels:
    * At least one successful pulse shape scan.

    - ∗ No saturation or underflow.
    - ∗ Successful fit.
    - ∗ Four different Bias settings employed (see table 2).
    - ∗ Correct Itp value reported and Peak $PulseHeight_2 >$ Peak $PulseHeight_1$.
    - ∗ Correct Vfs value reported and $Remainder_3 >$ 25ns $Remainder_2$.
    - ∗ Correct Vfp value reported and Peak $PulseHeight_4 >$ Peak $PulseHeight_3$.
    - ∗ Correct Vfp value reported and 25ns $Remainder_4 >$ 25ns $Remainder_3$.
  - The parameters that were extracted from the data for bias setting 1 were:
    - ∗ Average rise time over all channels (*trav*).
    - ∗ Average response time (t90) from all channels (*tresav*).
    - ∗ Minimum and maximum response time (*tresmin, tresmax*).
    - ∗ Remainder 25 ns after the peak (R).
    - ∗ Time of undershoot after the peak (Tu).
    - ∗ Depth of the undershoot (U).

- Pedestals and noise calibrations are performed with run 2. The signal to noise ratio is calculated from the ratio of the peak-pulse height to the noise.
- Gain Map with run 3 and 4.
- **Pipeline Cell**:
  - A cell is classified as dead if it possess a gain smaller than 60% of the average gain calculated for the chip.
  - The gain variation of a channel should not be more than 20% over the 187 pipeline columns.
  - The cell is deemed bad if the residual pedestal is greater than 2 times the channel noise. The residual pedestal is the average pedestal for each pipeline cell which remains after subtracting the average pedestal calculated for the readout channel and the linear common mode of 32 channels.
  - Every pipeline cell must have a relative gain > 0.6.
  - Gain variation along the pipeline within $<= \pm$ 20% .
  - Residual pedestal/noise $<= 2$.
- To obtain a value of zero in its status variable the chip had to pass the following cuts:
  - Average noise: $|70 \times Av_Noise - 1.3 \times PH_Ratio_Av - 36.75| \leq 12.25$.
  - Minimum noise: ≥ 0.6 ADC counts.
  - Rise time: $10 \leq trav \leq 20$ns.
  - Max-Min Response Time: ≤ 3ns.
  - Average Response Time:
Beetle 1.3/1.4: $|tresav - 50 + 0.25 \times PH_Ratio_Av| \leq 2.5$.
Beetle 1.5: $|tresav - 39.5| \leq 2.5$.
  - Remainder: $-0.3 \leq R \leq 0.1$ (All remainders).
  - Undershoot Time: $44 \leq tu \leq 70$ns (All undershoot times).
  - Undershoot: $-0.5 \leq U \leq -0.1$ (All undershoots).
  - This signal/noise cut means a noise-offset below $1200e-$ for all channels. Typical values then are below $900e-$.

The yield obtained from these cuts for each wafer is shown in table 3.2 which was obtained by monitoring the value of *status*. The total number of chips which are deemed to be good is 4325 with an average yield per wafer of 82.4%. The cuts presented in this section are not optimise and some variables are not included such as the registers or currents drawn on the chip. They do guarantee the functionality of the chip and the selection criteria hence the variable *status* is the first cut to be included in the VeLo selection criteria.

	Wafer Name	# Good Chips(%)
1	D2LI8FT	202(84.5)
2	D0LI9ZT	183(76.6)
3	D3LI8ET	197(84.2)
4	D3LI9WT	141(59.2)
5	D3LJ1ZT	227(95.0)
6	D6LI9TT	193(80.8)
7	D7LI7TT	219(92.4)
8	D7LI9ST	215(89.6)
9	D8LI7ST	216(90.0)
10	D9LI9ST	200(84.0)
11	DALI9PT	219(92.0)
12	DBLI7PT	220(92.1)
13	DDLI84T	210(87.9)
14	DELI7LT	204(85.7)
15	DFLI7KT	211(87.9)
16	DHLI80T	144(60.5)
17	DGLIA0T	226(94.2)
18	DKLJ9DT	216(90.4)
19	DNLI8UT	26(11.0)
20	DNLI9BT	219(92.0)
21	DPLI9AT	217(90.4)
22	DRLJ97T	220(91.7)
	Total:	4325(82.4)

Table 3: The yield of the 22 wafers, for which data is available, determined by the value of $status$. Due to the low yield of wafer 19, *DNLI8UT*, it was excluded from further studies.

4 VeLo Selection Criteria

The selection criteria described above is limited by not including cuts on the current drawn and also the characteristics of the Registers employed by the chip. Greater uniformity on the chips selected can be obtained if cuts are applied to the distributions obtained on all or the most important performance indicators of the chip. The large number of chips whose measurements are available makes this statistically meaningful. It also allows the extraction of the performance of a *typical* chip which is useful when understanding the performance of a chip being exercised.

4.1 Beetle Wafer Enlightenment

The main aim of the application, *Beetle Wafer Enlightenment*, is to facilitate the understanding on how the cuts placed on the variables affect the the yield and the large statistics help to gain insight into the performance of the front end. All the results to be presented in this report together with the graphs were produced with this application.

The application was written in C++ using Qt and ROOT libraries. It is able to read the wafer data, extract the variables on which cuts could either be enable or disable. The data for each variable is displayed as histograms, correlations between them, wafer maps and other functions for each wafer or for a selection of them. The graphs and yields are calculated in real time with only a few clicks necessary to display a histogram or correlation. Different Selection criteria can set, saved and compared.

The ability of the application to set the limits on the variables automatically is governed by equation 2. These set of equations employ the mean and the RMS of the distribution of the variable in question together a user set variable called $Yield_factor$. This variable is used to regulate the severity of the cuts on the variables.

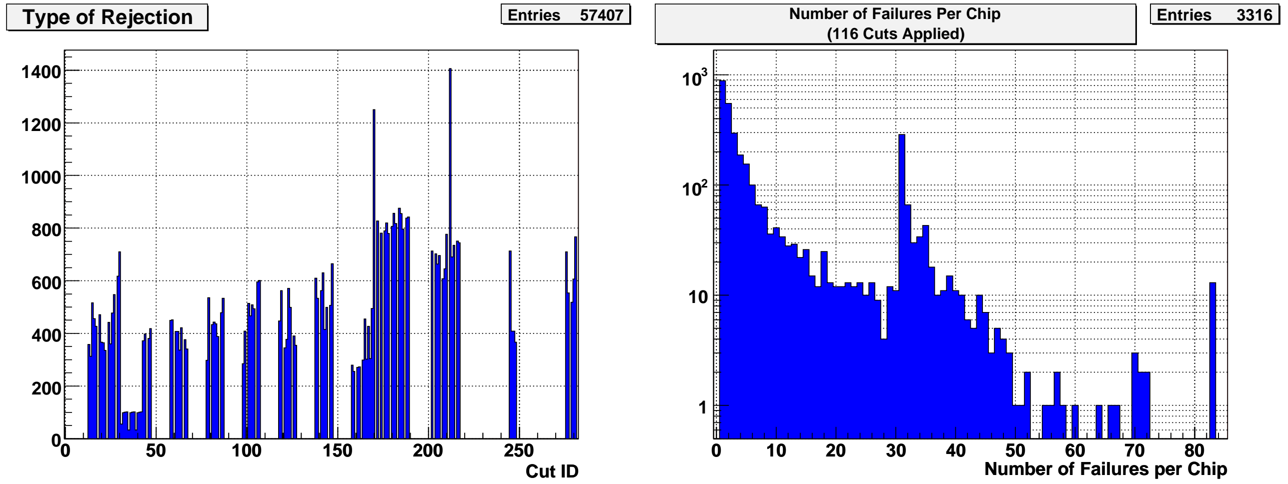

Figure 2: The histograms shows the number of times a certain cut a chip has failed and the number of cuts a chip has suffered. In the left, two cuts standout above the rest. These are the *Power On* current and the residual of the fit on the register *Isf*. The chips failing 30 cuts all came from the same wafer.

$$Low_Limit_{var} = Mean_{var} - Yield_factor \times RMS_{var} \quad (1)$$

$$High_Limit_{var} = Mean_{var} + Yield_factor \times RMS_{var} \quad (2)$$

4.2 The Variables

A first attempt to extract a yield by enabling all the variables available from the *adq* files was in the order of 10% percent. The histogram of a number of variables such as the *PowerOn* current still showed considerable tails even though the yield was low and the *Yield_factor* was set to 2.

Parameters extracted from the histograms were Mean, RMS and the Maximum and Minimum of the distribution. The irregular shape of the distributions prompted the to use arithmetic mean and RMS instead of fitting a function. Enabling all the variables resulted in a selection criteria that included more than 150 variables which included parameters for each variable for each bias setting. The low yield prompted careful review of the variable to select only applicable to VeLo operation and also to avoid over constraining the selection.

In figure 2 two histograms are shown. One histogram contains the ID of the variables which failed per chip and the other the number of cuts that the chip failed. The first one allows to see which are the most frequent variables that chip fail on and the second allows to judge whether it is more than one variable affecting the overall yield of the chips. The two variables that stand out from the first histogram is *Power On* current(ID 170) and the residual for the register *Isf* (ID 212). Each variable along is rejecting around 25% of the chips. The other two groups which claim a large number of chips are the rest of the variables associated with registers (ID 174 - 217) and the measurements performed at the four bias settings (ID 50 - 150). The left histogram shows that most of the chip are only rejected due to one or three variables. This points to the fact that a lot of failures seen on the histogram on the left are uncorrelated. The unusual peak at 32 rejections is mainly due to chips from one wafer. This could either be a bad wafer or the quality of the probing was different to the other wafers.

After carefully reviewing the variables the number which are included in the VeLo selection criteria was reduced. In table 4.2 the variables that are currently part of the selection criteria are listed. In the following section the variables were not included and the cuts modified are discussed.

Category	Variable	Remark
Current(I)	Mean Reset (S0) Mean Operating (S0)	Chips should draw similar currents.
Headers	Cross Talk Amplitude Mean Amplitude RMS	All four port included. All four ports included. All four ports included.
Res Pedestal/Noise	Mean RMS	Initialised with S1 Initialised with S1
Relative Gain	Mean RMS	Initialised with S1. Initialised with S1.
S/N Performance	Mean RMS	initialised with S1. Initialised with S1.
Pulse Scan	IPT VFP VFS	S1,S2,S3 and S4 included. S1,S2,S3 and S4 included. S1,S2,S3 and S4 included.
Peak PH	Mean RMS $\mathrm{Mean}_{S2}/\mathrm{Mean}_{S1}$	Only S4 included. Only S4 included. Reject low gain chips.
25ns Remainder/Peak Height	Mean RMS	Only S4 included. Only S4 included.
Pulse Response Time (t90)	Mean RMS	Only S4 included. Only S4 included.
Pulse Rise Time t(90-10)	Mean RMS	Only S4 included. Only S4 included.
Undershoot − Peak Time	Mean RMS	Only S4 included. Only S4 included.
Undershoot/Peak Height	Mean RMS	Only S4 included. Only S4 included.
Registers	IVoltBuf Grad IVoltBuf Residual IVoltBuf MaxVal	Quadratic Fit
	Itp Grad Itp Residual Itp MaxVal	Linear Fit
	Isha Grad Isha Residual Isha MaxVal	Quadratic Fit
	Isf Grad Isf Residual Isf MaxVal	Linear Fit
	Icurrbuf Grad Icurrbuf Residual Icurrbuf MaxVal	Linear Fit
	Ipre Grad Ipre Residual Ipre MaxVal	Linear Fit
	Ipipe Grad Ipipe Residual Ipipe MaxVal	Quadratic Fit
	Ibuf Grad Ibuf Residual Ibuf MaxVal	Linear Fit

Table 4: The 69 variables used for the VeLo selection criteria together with *status*.

4.3 Reviewed Variables

In this section the variables that adversely affected the yield or showed some kind of anomaly in their distributions are discussed. The aim was to understand the cause and develop a strategy that would result in increasing the yield without compromising the selection criteria.

4.3.1 Power On Current

The variable that was responsible for the greatest number of rejected chips was the mean of the *Power On* current. Its distributions (the first graph shown in figure 3) clearly shows the reason for the high number of rejection and the long tails after the cut has been applied. There is a distinctive cluster of chips with high current that have formed a small secondary peak next to the main distribution. This second peak contain a few hundred chips which should be rejected but has increased the value of the RMS allowing the cut also include a number of these chips.

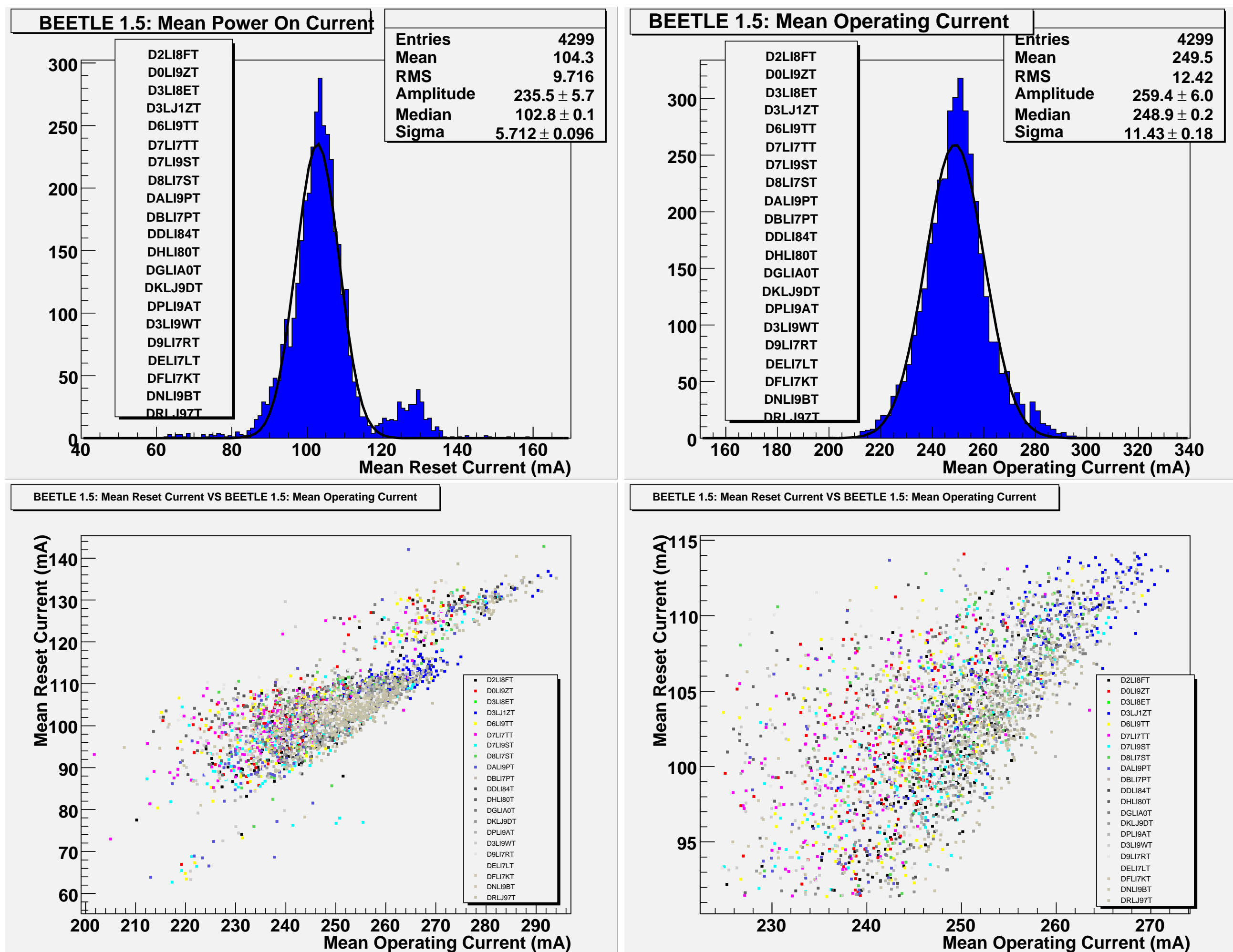

Figure 3: These are the distributions of the two currents which are measured during the wafer probing. The first two distributions have no cuts applied (except the status variable) and the difference between the two can be easily seen. The *Power On Current* features a small second peak which increases the mean and the RMS. A fit was employed and the parameters extracted where used to define the cut (*factor=2*). The last figure shows a much cleaner correlation which is obtained after the two cuts are applied. The resulting yield is 3237 which corresponds to 75%.

Mean	Bias Setting 1	Bias Setting 4
Pulse Peak Height(ADC)	39.35 ± 0.65	40.84 ± 0.63
Pulse Response Time(ns)	14.35 ± 0.55	15.39 ± 0.51
Pulse Rise Time(ns)	54.41 ± 2.1	71.30 ± 2.40
25ns Remainder/PeakHeight	-0.127 ± 0.021	0.158 ± 0.024
Undershoot - PeakTime(ADC)	54.64 ± 0.67	64.42 ± 0.91
Undershoot/PeakHeight	-0.2741 ± 0.0162	-0.1076 ± 0.0049

Table 5: The mean and the RMS of the distributions obtained for the default and VeLo bias settings using all the chips that passed the *status* cut. The different RMS values contributed to increasing proportion of chips rejected hence only measurements on bias setting 4 were included in the selection criteria. The small RMS obtained for the *Undershoot/PeakHeight* is artificial and due to poor binning that resulted on a large number of chips having the same value for the ratio.

Interestingly the distribution obtained for the mean *Operating* current does not show such distinctive peak but the correlation between the two variables exhibits an island featuring chips with high values for both currents. From this it can be concluded that the effect is real and the chips should be rejected. For the *Power On* current instead of cutting on the RMS of the distribution a Gaussian fit on the main peak would be a more appropriate method to extract the required parameters for the rejection. Hence for the VeLo selection criteria the mean of the *Power On* current was employed 102.8mA and a sigma of 5.712mA.

The fourth graph featured in figure 3 shows the correlation with the updated cuts for the *Power On* and *Operational* current set with a *Yield_factor* of 2. The correlation is missing the high current island and any low current chips. The number of rejected chips still high with the fraction being around around 25% (3237) but now the correct chips are being rejected.

4.3.2 The Bias Setting Measurements: Correlations

Another source of rejection that required attention was the multiple cuts applied to the the values extracted as the chip was operated under different bias settings. It was expected since it is the same circuitry that the rejections would be at some level correlated.

When applying cuts, a total of 25, on bias settings 1 and 4 separately the yield obtained was 2237(44.6%) and 2436(48.6%) respectively. In each case cuts were also applied on the reported bias settings to ensure that the correct values were applied. It was expected that the mean of the parameters extracted for the different bias settings were correlated. This is shown in figure 4 where the correlation of the mean *Pulse Height* and the mean *Undershoot/PeakHeight* ratio. The first three graphs show the correlation of the mean *Pulse Height* between bias setting 1 and 4. The data for each graph was subjected to different cuts. Only a cut on *status* was applied for the data shown on the top left graph while the top right graph included setting 4 cuts and the bottom left included setting 1 and 4. Collectively the graphs show that a linear correlation does hold for the complete range of pulse height measured. This was true for all the variables measured under different bias settings except for the mean of the *Undershoot/PeakHeight*. The bottom right graph shows a value for the ratio measured under setting 4 is more prevalent than others. The prevalent value centred between -0.115 and -0.110. This is created by the width of the bins of the histogram in the *adq* file causing the measurement from all the channels to fall within one bin for setting 4 *Undershoot/PeakHeight* measurements.

Even though the mean of the results from the two bias setting are correlated their distributions have different widths. The RMS for the distributions are shown in table 4.3.2 with the RMS for the *Undershoot/PeakHeight* distribution being artificially low due the problem previously outlined. This difference in RMS resulted in chip being rejected when both set of cuts were applied even though they have passed one set and thus guaranteeing their functionality and performance (as long as registers are also scrutinised). The yield with the two set of cuts applied decreased to a value of 38.3% (1922 chips) and hence it was decided that cuts were only be applied to bias setting 4 measurements.

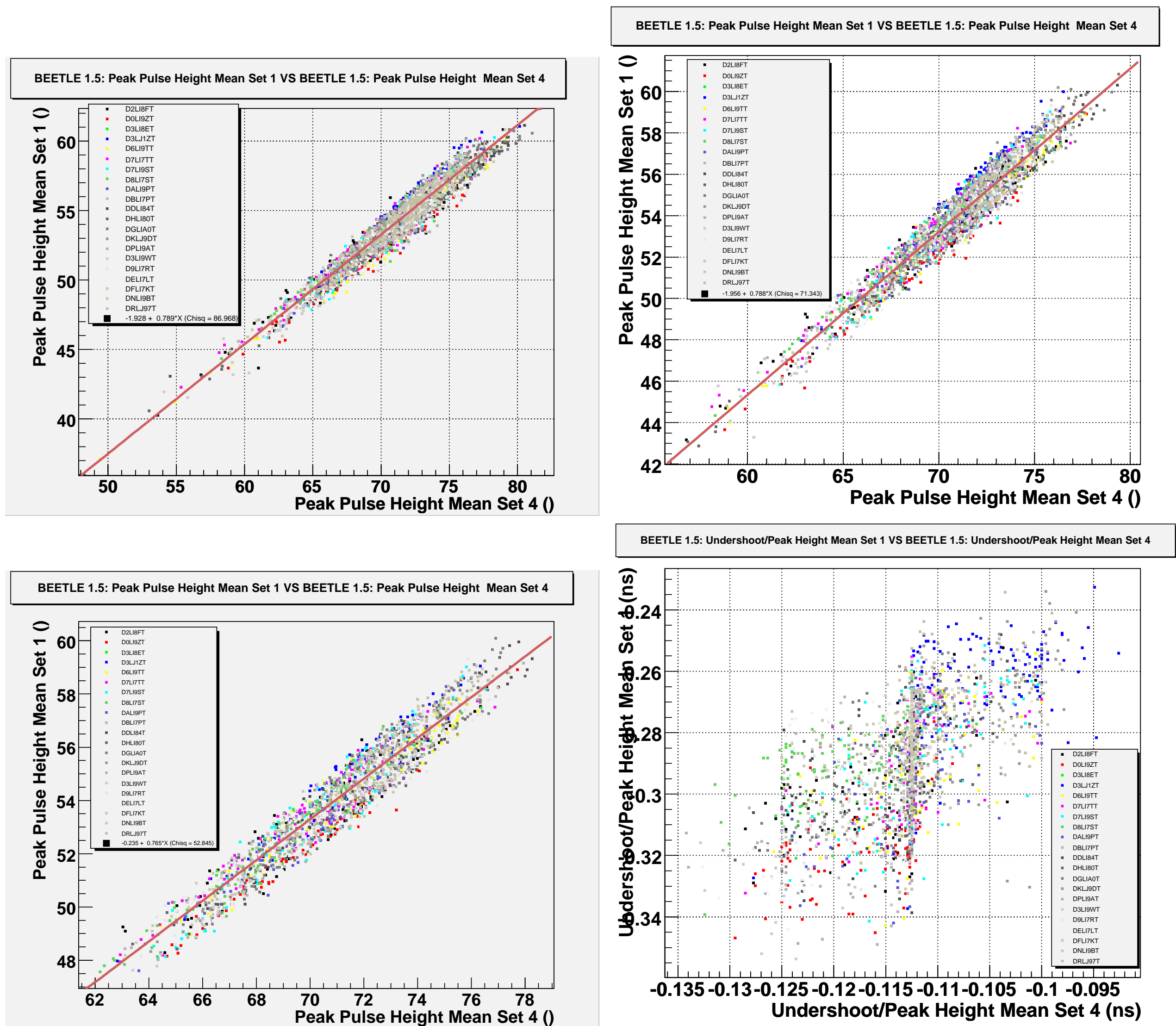

Figure 4: The correlation between the Peak Pulse Height measured with Setting 1 and Setting 4. The first graph was obtained with no cuts related to the settings applied shows the correlation of the mean between the settings. The two other graphs shows the same correlation after S4 cuts are applied and S1 and S4 cuts are applied. The last graph shows the mean for the undershoot PeakTime which seems to have a much weaker correlation. This is due to the binning which was not optimum for Setting 4 and hence the large values with the same mean.

4.3.3 The Bias Setting Measurements: Gain distribution

An important point that can be explored with the measurements performed under different bias settings is the gain of the chip. This is achieved by comparing the mean *Pulse Height* obtained for settings 1 and 2. The only difference between the two settings is the value of *itp*, 22 and 34 respectively, thus making it a direct measurement of the gain of the chip. In figure 5 the ratio of the two means is shown.

A feature of the distribution shown in figure 5 is its asymmetry after 25 cuts have been applied to the chip sample. The asymmetry featured is a tail extending the low end of the distribution. The consequence is that there are low gain chips, as much as 100, that are being included in the selected sample. To avoid polluting our sample a new variable, PH_{S2}/PH_{S1},

was defined within BEW. The limits applied to this variable were derived from 1.525 ± 0.014. This was extracted from a Gaussian fit to the distribution shown in figure 5 rather than calculating an arithmetic mean because the increase to the RMS due to the tail.

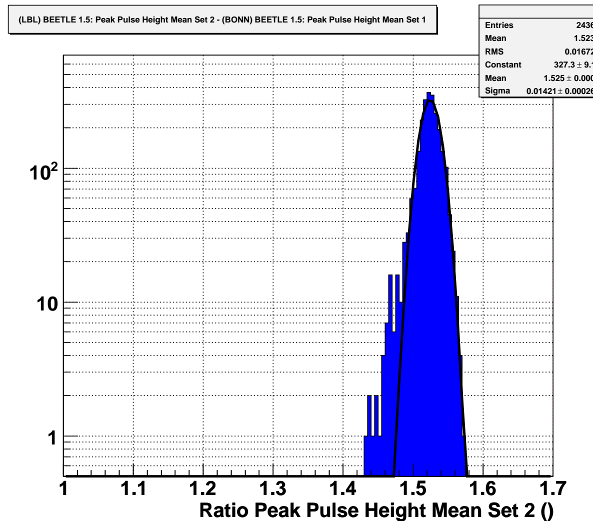

Figure 5: The ratio of Pulse Height between bias setting 2 and 1. The low gain chips that contribute to the tail of the distribution prompted the definition of a new variable so that a cut to be applied to it. The cut was based on the parameters extracted from the Gaussian fit rather than the arithmetic mean.

4.3.4 The Bias Setting Measurements: Asymmetrical cuts

A number of variables measured as part of the bias setting measurement prompted application of asymmetrical cuts to their variables. The reason for this was that there was no reason to reject chip that were better than the average for certain properties. The variables that were considered to be part of this category were related to the remainder of the pulse and the overshoot. These are listed here:

- **25ns Remainder/Peak Height Mean**: The VeLo bias setting result on this value being positive but the smaller the ratio the pulse is recovering. This prompted the decision to always set the lower limit to 0 as there is no reason for rejecting chip of such quality.
- **Undershoot - Peak Time Mean**: This value is another measurement of how fast the pulse is recovering and as in the previous case there is no reason to reject chips on the low end of the distribution. The low limit for this variable was set to 55 which is 5sigmas away from the mean.
- **Undershoot/Peak Height Mean**: This is a negative value as the sign of the undershoot is negative. The smaller the magnitude of this ratio the faster the pulse will approach the baseline. As in the two previous cases this prompted an asymmetric cut but this time to include chip in the high end of the distribution. The high limit that was always set for this variable is -0.05.

The result of this amendment to the selection criteria was slight with the yield increasing only by a handful of chips.

4.3.5 The Beetle Registers

Another source of chip rejection, as shown by the first graph of figure 2, were the variables associated with the characterisation of the *Beetle* registers. The characterisation involved measuring the output of the register for a number of dac values.

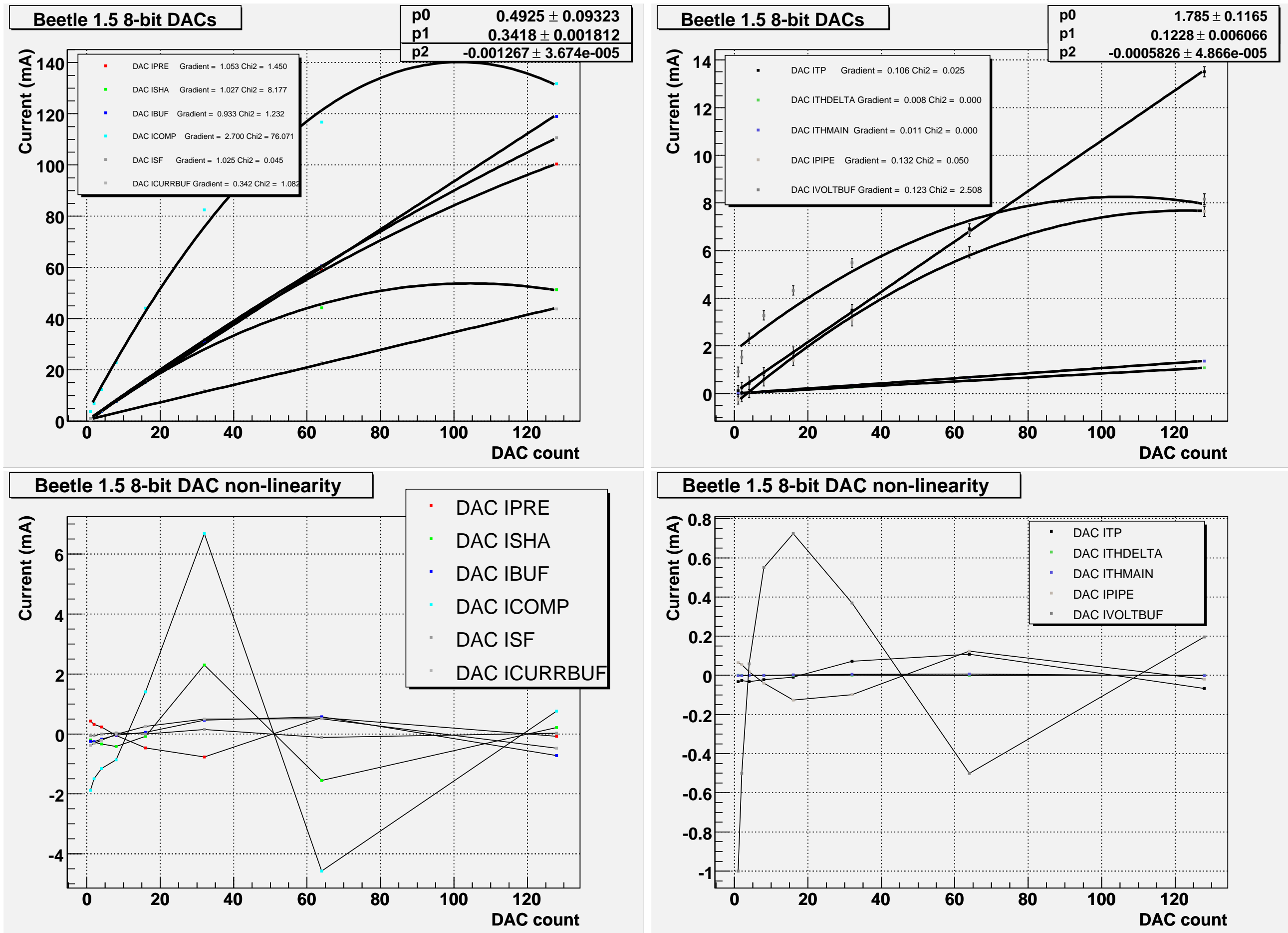

Figure 6: The Beetle registers which are relevant to the operation of the VeLo. The output of the registers was measured by setting only one bit at a time(1,2,4,8,16,32,64,127). Depending on the register the output was fitted with a line or a quadratic function. The bottom graphs show the measured residual for each register.

These were strategically chosen so that each of the 8-bits composing the dac were set high. Hence for each register the dac measurement included 1,2,4,8,16,32,64 as well as 127 to measure the full output of the register. In figure 6 the two top graphs show the 11 measured registers for a typical *beetle* chip.

There are two motivational issues for the reason of performing the dac characterisation. The first one is exercise the complete range of the dac to guarantee that there has not been any point defects during the wafer processing that would result in a certain dac bit being corrupted. That is a bit that is always set high or low and thus disrupting the continuity and granularity of the dac. The second issue is due to the fact that the output of the registers, because they are biasing the chip, play an important part on its performance. The characterisation allows the possibility for compensating for the difference in a chip to chip basis. For this not be necessary or a second order effect the parameters describing the performance of the registers should also be part of the selection criteria in an effort to obtain a uniform batch of chips.

For each register four parameters were extracted from the measurements. These were:

- *Gradient*: The change in current per dac value.
- *Constant*: The position where the line crosses the y axis.
- *Residual*: The sum over all the measurements of the difference squared between the measured and fitted output.

- *Maximum Output*: This was the measured value when all the bits of the register were set.

This assumed that the registers are linear but an striking aspect of 6 is that there are four registers which are not. These four registers were fitted with a quadratic function to keep the *residual* a meaningful variable. The quadratic constant became the fifth parameter to be extracted from the measurements. The bottom graphs of figure 6 show the resulting difference between the fitted function and the measured output as a function of dac value. The small differences show that in most cases the chosen function does describe the register although the description and fitting would benefit from a greater number of measured points. The register with the highest difference is *Icomp* but together with *Iththeta* and *Ithmain* are not employed during the VeLo mode of operation hence they will not be included in the study.

To reject chips with failing bits in registers such as the example one shown in figure 7 there were two strategies put in place. The first one was to place cuts on the gradients and residuals. The second involved the practice of multiplying the gradient by a factor of -1 if the output of the register was equal to zero for any dac setting tested. This was necessary because the output of a small register settings such as 2, 1 or 4 would not influence the fit nor increase the residual to a high and distinctive value. The -1 factor would ensure the gradient be outside the range of the cuts. Cuts were placed on *Maximum Output* value as well but the quadratic constant and the offset of the function were exempt because of their small contribution to the overall register output.

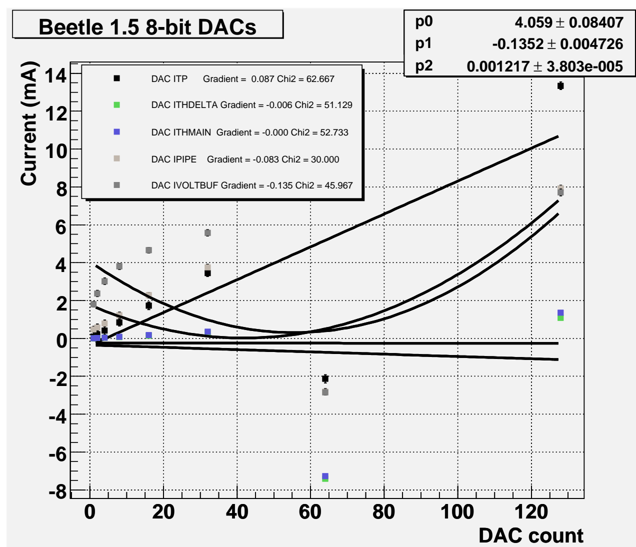

Figure 7: A chip whose register is corrupted.

5 Yield vs Factor

In total 70 cuts were included in the VeLo selection criteria. Their values were obtained from their own distribution except in the cases previously mentioned. To understand how the total of 70 cuts affected the yield the value of *Yield_factor* (see equation 2) was changed and the resulting graph is shown in figure 8. Choosing a value of 2.8 seems to yield enough chips ($\approx$ 2000) for the complete VeLo production and a generous overhead without compromising the functionality and performance of the chosen chips.

6 A typical Beetle 1.5 chip

One bi-product of placing such detailed selection criteria on a large sample of chips is that the performance of the typical *beetle* can be specified. The values are extracted from the resulting distributions after all the cuts were placed with the

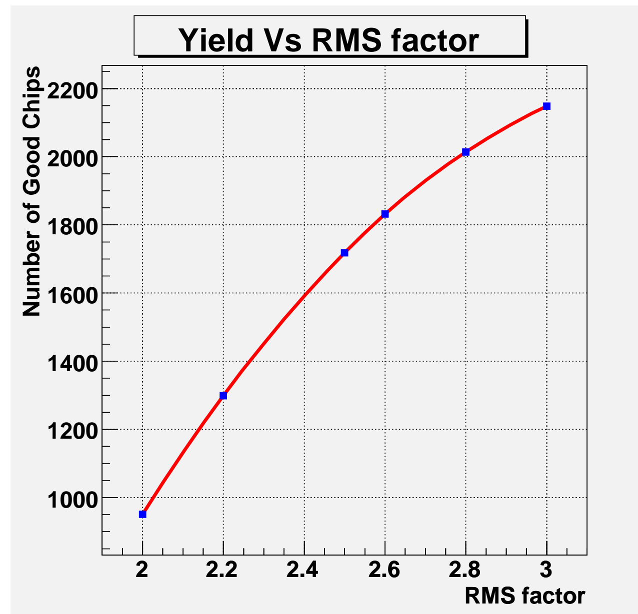

Figure 8: The number of good chips that passed the 70 cuts as a function of RMS factor or Yield factor.

selected *Yield_factor* (2.8). The performance of the chip is summarised in table 6 with values associated with the *Beetle* registers listed in table 6. A curious thing is the value of the *xtalk* for port 1 which remarkably different from the rest of the ports.

7 Conclusion

The aim for developing a VeLo selection criteria was to choose chips in terms of their functionality and performance. Variables were incorporated which reflected the performance and functionality that is required for VeLo operation. The range of the cuts was derived from the distribution obtained from the measurements performed during the wafer probing. The nature of the distributions meant that parameters extracted were the mean and rms instead from Gaussian fits except for the variables discussed in the text. The starting point for the criteria was the variable *status* and 69 others were applied to the batch of chips that pass this first cut. The selection criteria, with a *Yield_factor* set to 2.8, selected 2014(42%) chips which is a more than an adequate number to complete the VeLo detector.

References

[1] LHCb VeLo Technical Design Report, CERN/LHCC 2001-011.

[2] N. Van backel etal *The Beetle Reference Manual* Electronics, LHCb 2005-105.

[3] J. Blouw Description of Wafer probing measurements, private communication.

Category	Variable	Value		
Current(mA) S1, Fit	Power	103.2	±	5.5
	Mean Operating	250.7	±	7.9
Header XTalk(%)	Port 1	1.806	±	0.595
	Port 2	4.253	±	0.293
	Port 3	3.883	±	0.170
	Port 4	3.392	±	0.141
Header Amplitude (ADC)	Mean Port 1	67.67	±	3.00
	RMS Port 1	0.133	±	0.030
	Mean Port 2	65.29	±	3.23
	RMS Port 2	0.112	±	0.027
	Mean Port 3	64.72	±	3.17
	RMS Port 3	0.098	±	0.028
	Mean Port 4	64.65	±	3.24
	RMS Port 4	0.105	±	0.028
Residual Pedestal/Noise(S1)	Mean	(-1.89	±	184.00)$\times 10^{-06}$
	RMS	0.157	±	0.014
Relative Gain(S1)	Mean	1..00	±	0.00022
	RMS	0.0128	±	0.0014
S/N Performance(S1)	Mean	35.66	±	1.45
	RMS	1.25	±	0.34
Peak Pulse Height Setting 4(ADC)	Mean	71.64	±	2.92
	RMS	2.41	±	0.93
	$Mean_{S2}/Mean_{S1}$	1.523	±	0.015
25ns Remainder/Peak Height	Mean	0.135	±	0.032
	RMS	0.0116	±	0.0043
Pulse Response Time (t90) ns	Mean	40.78	±	0.80
	RMS	0.297	±	0.123
Pulse Rise Time t(90-10) ns	Mean	15.41	±	0.67
	RMS	0.304	±	0.130
Undershoot − Peak Time ns	Mean	62.79	±	1.70
	RMS	1.14	±	0.46
Undershoot/Peak Height	Mean	-0.113	±	0.00646
	RMS	0.007151	±	0.004889

Table 6: The performance in numbers of a typical Beetle 1.5 FE. The mean values for all the variables that are part of the selection criteria except for the registers(See table 6. These were extracted from the distributions that only included chips selected.

Beetle Registers				
Register	Quad(mA/DAC^2)	Gradient(mA/DAC)	Residual(mA^2)	Maximum Output(mA)
IVoltBuf	$(-56.0 \pm 5.84)\times10^{-5}$	0.115 ± 0.011	2.036 ± 0.305	7.31 ± 0.54
Itp		0.106 ± 0.0015	0.0182 ± 0.0046	13.55 ± 0.19
Isha	$(-48.3 \pm 1.04)\times10^{-4}$	1.006 ± 0.016	9.086 ± 1.697	50.00 ± 0.75
Isf		1.014 ± 0.032	0.321 ± 0.533	103.50 ± 10.95
Icurrbuf		0.339 ± 0.006	1.20 ± 0.29	43.50 ± 0.80
Ipre	$(-2.0 \pm 0.12)\times10^{-3}$	1.03 ± 0.02	1.40 ± 0.27	97.12 ± 1.34
Ipipe	$(-54.9 \pm 1.45)\times10^{-5}$	0.133 ± 0.0023	0.047 ± 0.0080	7.81 ± 0.18
Ibuf		0.908 ± 0.0145	1.674 ± 0.5473	116.10 ± 1.86

Table 7: The mean characteristics of the Beetle registers that were included in the selection criteria. The term *Quad* refers to the quadratic term of the quadratic function that was used to fit the measurements of the register. Residual is the sum of the difference squared between the measured value and the result from the fit for a given DAC. The sum is over all the DAC values sampled.