SCT interlock specifications

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SCT interlock specifications

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Introduction

An hard wire interlock system will be implemented between the detector cooling system and the power supplies and between the readout system and the power supplies. The interlock on the cooling system will protect the silicon detectors for over temperature while the redout interlock will protect the operator for laser light when the data fibres are disconnected from the receiver boards. The components of the interlock system will be described in this document.

Description of the system

The temperature of the cooling pipe next to the last silicon detector module on the cooling loop is sensed. If the mass flow of coolant is too low to cool all silicon detector modules the last module on the cooling loop will be the first to sense the anomaly. High temperature at the last module will trigger the power to be switched of for all silicon detectors in that loop. A cooling loop is defined as having an independent injector for coolant while the exhaust can be manifolded. In Barrel SCT a cooling unit, schematically drawn in figure 1, contains two cooling loop with 24 silicon detector modules each. The End Cap SCT has three types of cooling units. The cooling units with three loops, schematically drawn in figure 2, are on disks 1,2,3,4,5 with 14 silicon detector modules on the loop at the largest radius and 10 silicon detector modules on the two other cooling loops. Disks 0, 6 and 7 have two cooling loops per unit and disk 8 has only one.

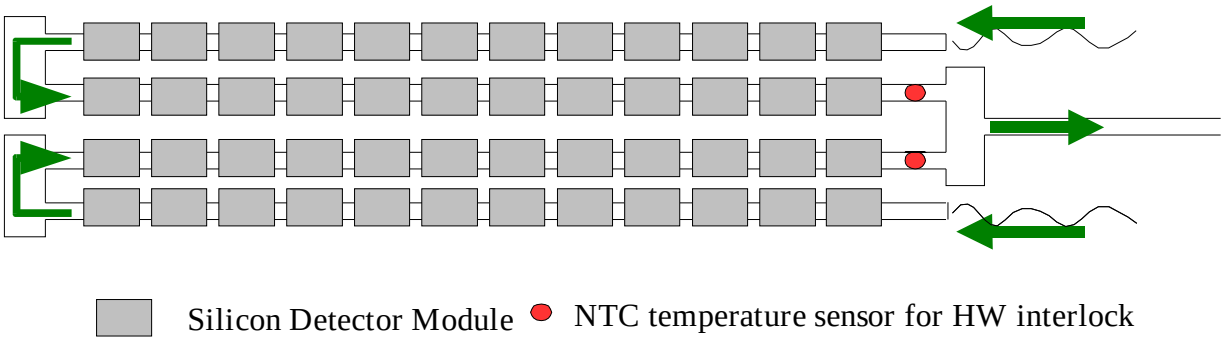

Figure 1. Barrel cooling unit.

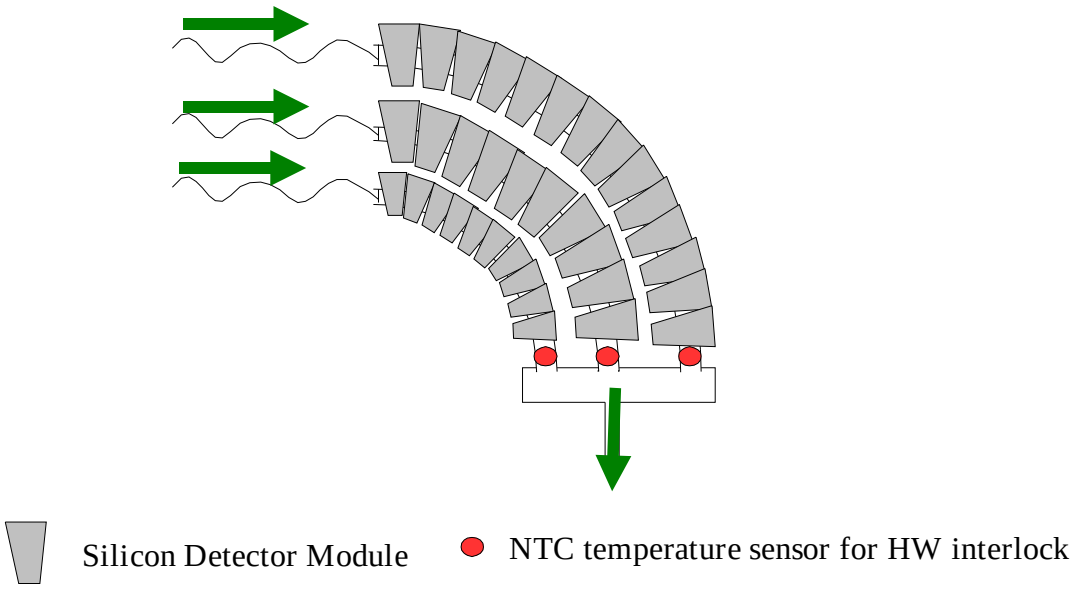

Figure 2. EC cooling unit for a quarter disk.

The NTC thermistor is connected to an ELMB and a interlock box (IBOX) at the DCS service box accessible in the UX cavern. To prevent a failure of a single thermistor each thermistor is doubled on the cooling tube but only one is connected to the IBOX. If the first thermistor fails the input to the IBOX can be replaced by the second thermistor. The ELMB monitors the temperature of the NTC and sends the values over CAN−bus to the DCS software. The IBOX has a fixed threshold and high temperature flips a bit on the output of the IBOX which is sent over a parallel bus to the interlock matrix (MX) located in service caverns US15/USA15 near the power supplies. The IM associates the power supply channels to the correct cooling loop and connects to the power supplies over a crate interlock card (CIC) over a 13 line bus. Figure 3 shows a schematic drawing of the temperature interlock.
The interlock for the optical fibres is trigged by opening the the door to the BOC card. The signal will be routed via the MX and the CIC to the power supplies switching off the current to the VCEL.

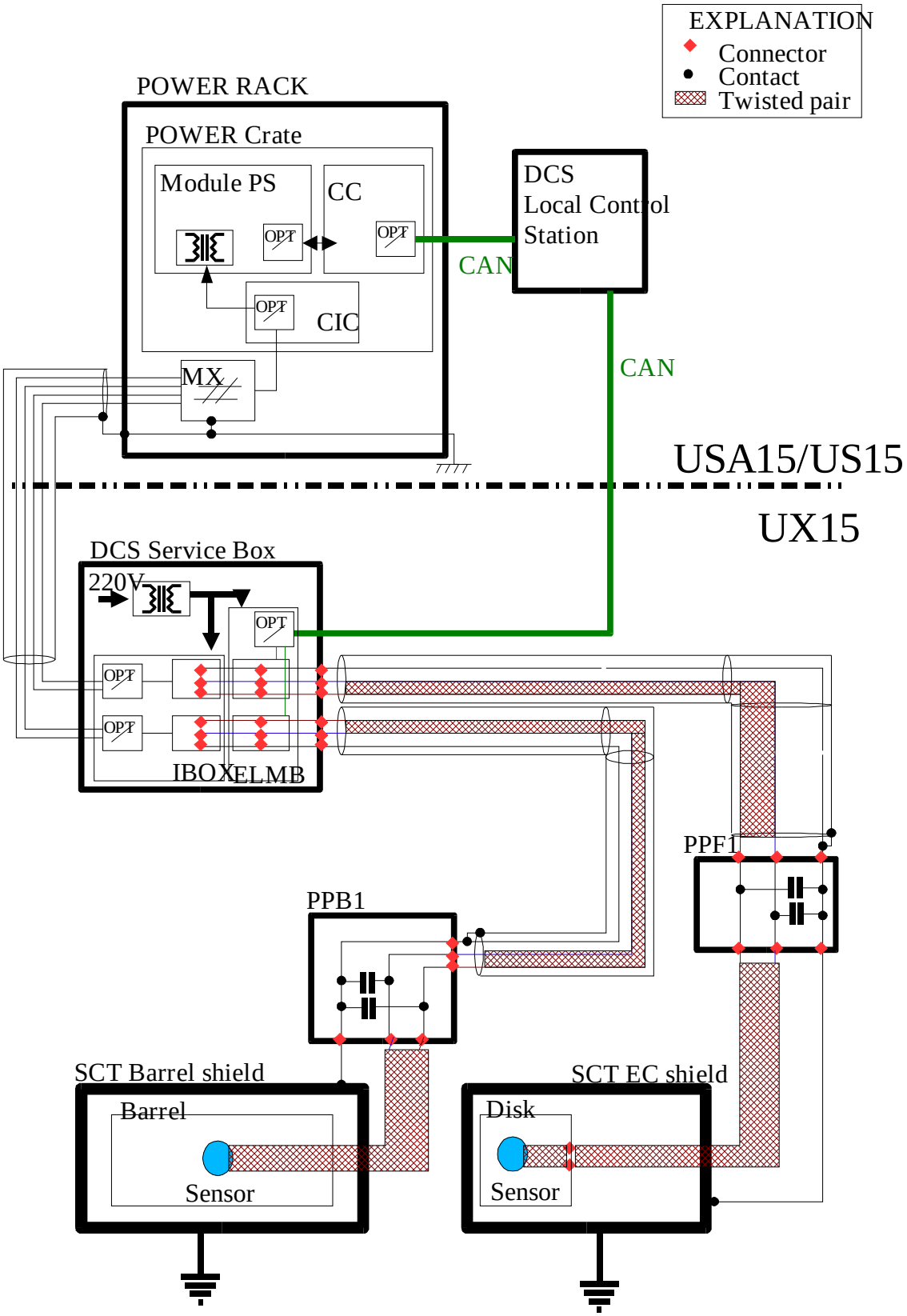

Figure 3. Temperature interlock circuit.

Interlock architecture

The power supply channels are mapped to the correct cooling tubes by MX. The silicon detector modules in the barrel are powered from both +Z and −Z side while the cooling is will flow on both the +Z and −Z side. This adds complexity because the detector modules on +Z and −Z sides are not necessarily powered from the same crate. One power supply crate powers four half−cooling loops. Assuming the power distributed from different crates to +Z and −Z sides one crate with 12 4 channel Low Voltage cards receives input from 4 thermistors.

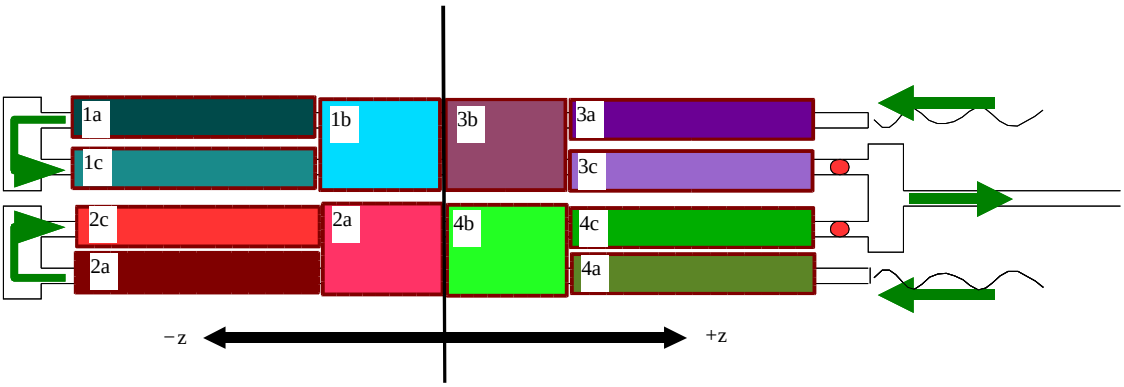

Figure 4. Mapping of detector modules to power supply in Barrel.

The EC SCT has not the problem of electrical separation which makes the interlock logic simpler. A three loop cooling unit has 14+10+10 = 34 silicon detector modules requiring 10, a two loop cooling unit require 7 and a one loop unit requires 3 Low Voltage cards correspondingly.

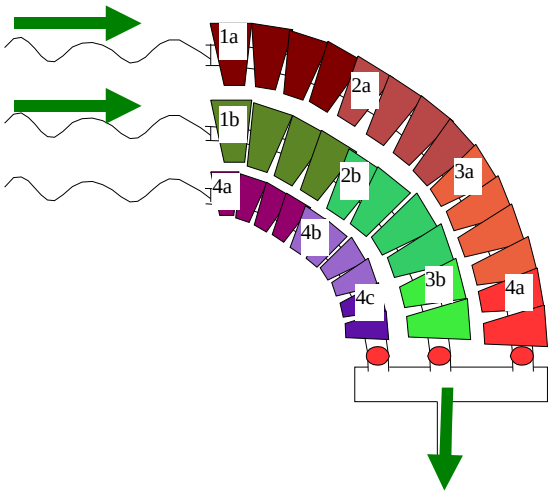

Figure 5. Mapping of detector modules to power supply in EC.

The SCT DCS services are grouped in quadrants and therefore the interlock is naturally grouped accordingly. The Barrel and The EC services are routed to the same SCT DCS service platform but have independent electronics. The maximum number of thermistors included in the interlock by a quadrant are 14 for the barrel and 28 for the EC.

Interlock Box (IBOX)

The IBOX was originally developed for the ATLAS Pixel Detector but will be now used by several sub−detectors in ATLAS. The functionality of the IBOX is described in ref [1],[2]. The IBOX is designed for 16 NTC thermistors with two wire connection. The device has two logic outputs that can be used to indicate in addition proper working condition high temperature, low temperature and sensor error. The IBOX will be connected in parallel with a ELMB allowing the temperature to be monitored by the DCS software. In the parallel configuration the thermistor is biased by the IBOX and the ELMB sense the temperature entering the IBOX. The IBOX a single +5 V supply. The NTC thermistor is supplied via a 66 kΩ resistor from a +2.5V supply. The output logic is in high state (+5V) when in normal operation and in low state (0V) when interlock is trigged by high temperature. If the power is lost to the IBOX all output channels are low which will switch off all related power supply channels.
The output of the IBOX will be opto coupled by a separate board. (Append circuit diagram and schematics)

Signal on input

- Differential NTC signal.

Signal on output

- Interlock active "LOW" = 0V (GND).
- Interlock inactive ”HIGH” = +5V.

Input connector

- 20 pin IDC .

Output connector

- 34 pin IDC .

Power

- +5V, GND.

Size

- 3U

Interlock Matrix (MX)

The MX will have 28 temperature interlock and 1 opto−interlock input lines. The MX has 10 groups with 12+1 output lines.

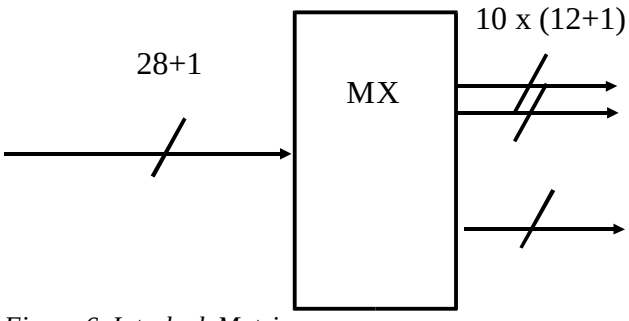

Figure 6. Interlock Matrix

Crate Interlock Card (CIC)

The CIC receives 12 temperature interlock signals and 1 opto interlock signal from MX. The CIC isolates electrically the power supply crate from the interlock system with opto couplers. The 12 input lines are routed via the CIC to power supplies over the crate back plane. The circuit on the CIC comprises a opto coupler, a inverting Schmitt trigger and a Darlington driver. The Darlington driver receive its bias current from the power supply.

Signal on input

2. Interlock active ”LOW” = 0V (GND).
3. Interlock inactive ”HIGH” = +5V.
4. Rise time 1 ms −10 ms.

Signal on output

- Interlock active "HIGH" = 5V
- Interlock inactive "LOW" = 0V

Input connector:

9 DB15 male from MX to the crate backplane.

pin 1 and 15 = GND
pin 2 to 13= LVILOCK0 − LVILOCK11
pin 14 = ILOCKGLOBAL

- 96 pin connector from crate backplane to the interlock card.

Output connector

10 96 pin connector from the interlock card to the crate backplane.

row c, pin 27 to 32 = LVILOCK0 − LVILOCK5
row a, pin 27 to 32 = LVILOCK11 – LVILOCK6
row c, pin 26 = ILOCKBLOBAL

Power

11 From the backplane of the crate through the 96 pin connector.

row b, pin 32 = +5 V
row b, pin 23 = GND

Circuit on board (13 channels)

9 Driver for single−ended interlock signal for both LED indicator and opto−coupler.
10 LED indicator for interlock inactive state.
11 Opto−couplers on the input of the interlock card, failure mode “LOW”.

Size

11 3U.

Reference

[1] Susanne KERSTEN, Requirements for the Interlock Circuit and System of the ATLAS Pixel Detector, ATL−IP−ES−0040

[2] Susanne KERSTEN and Peter Kind, Technical Description of the Interlock Circuit and System for the ATLAS Pixel Detector , ATL−IP−ES−0041

Appendix 1 (CIC−schematics and layout)

EDMS: ATL−IS−ED−0005 v.1,

https://edms.cern.ch/cedar/plsql/doc.info?cookie=1692961&document_id=331408&version=1