The Semiconductor Tracker Detector Control System Requirements Document

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1 Preface

   This document is planned to become an appendix to the "ATLAS Detector Control System User Requirement Document"[1]. The requirements are written in the same format as in the main document. This document is the result of discussions on the ATLAS SCT DCS held the 18. October 1996 at CERN. There may be requirements that will be removed from this document because the part they describe doesn't belong the DCS. A requirement number (eg. SCT−LV1) for a deleted requirement will not be taken by a new requirement. There has been requirements added to the document. New requirements added or requirements which have been modified since draft 1.1 are flagged with ☑ and ☒ correspondingly. The "Introduction" and the "Definition" part has been enhanced with a text prepared by Serege Basiladze.

2 Introduction

1. The detector control subsystem for the SemiConductor Tracker (SCT) operates and supervises the SCT subdetector and its infrastructure.

2. The subsystem is one of several parts of the ATLAS Detector Control System (DCS). The general DCS requirements are defined in the ATLAS DCS Users Requirements (UR) Document[1].

3. The main functions of the SCT DCS subsystem are:

• monitoring	*read−out of analogue and digital status signals;*
• diagnose	*send test signals to components in the subsystem and analysis of the response;*
• control	*distribution of necessary analogue and digital status signals;*
• interface	*making the SCT DCS subsystem available for the user, ATLAS DCS and the DAQ;*
• logging	*logging data from the SCT DCS subsystem;*

4. The subsystem shall perform to detect 3 categories of anomalies with estimated time spectrum:

• ultra−slow variations of parameters caused by ageing, radiation damage etc.;	1−10a
• climatic variations caused by fluctuations of temperature, humidity, air pressure, etc.;	1−100h
• electrical variation caused by defects in power supplies or influence of external power setups, etc.;	1−100ms

2.1 The main components of the SCT DCS subsystem

1. The DCS for SCT include the following parts:

- Subdetector status monitoring;
- Low Voltage power supply control and monitoring;
- High Voltage power supply control and monitoring;
- Cooling control and monitoring;
- Alignment system;
- Monitoring of environment parameters.

2. The data from the DCS is subdivided in two groups:

- Safety information;
- Parameters valid for physics data.

3 Definitions

1. The main components of the SCT subdetector is described for the user in a hierarchial structure which consists of 4 layers:

- SCT subdetector   *a part of the ATLAS Inner Detector located between the Pixel subdetector and the Transition Radiation Tracker;*

- section   *a (repetitive) part of the SCT subdetector which can be installed and operated as one unit (a cylinder in the barrel or a disk in the forward detector);*

- sector   *a part of the barrel layer or a part of the disk which can be operated autonomously (a stave in the barrel);*

- module   *an element (the smallest part) of the sector, silicon sensors with hybrids and readout electronics. Up to 10−12 modules/sector;*

2. The logical structure of the SCT DCS subsystem corresponds to the main layers of the SCT subdetector and is subdivided into *(see fig. 2 in the ATLAS URD [1])*:

- SCT DCS subsystem   *a subdetector layer in the ATLAS DCS which has a certain autonomy with only loose connections to other subsystems in ATLAS;*

- node   *a (repetitive) part of subcomponent to the section in the SCT;*

- unit   a *functional element of node, corresponds to a module in the SCT;*

- send/act   *sensors and actuator on sub− or zero layer;*

3. The logical structure shall be used for the definitions of names for the subdetector and subsystem parts in according to general DCS agreement.

4. The following names explained below will be used in the requirements.

- powersupply crate   *an unit consisting of a crate controller and several power blocks;*

- crate controller   *an interface between the DCS bus on one hand and the internal crate bus on the other hand. The crate controller has a microprocessor and memory;*

- power block   *a card with power supplies for several modules and connection to the hardwired interlock bus;*

5. The user requirements are qualified with the following attributes:

Need:	Level of importance	
essential:	must be implemented	
desirable:	should be implemented if not too difficult	
optional:	would be nice to have	

Priority:	for incremental delivery of DCS	
Phase I:	stand−alone operation with reduced functionality	
Phase II:	Final system with integrated operation	

Stability:	indicates whether the requirement is expected to change	
stable:	is not expected to change	
tbc:	to be confirmed, might not be needed	

Source:	who has asked for this requirement	
general:	needed by most users	
DCS:	requested by DCS	
SCT:	requested by SCT	

4 Requirements

4.1 Control and monitoring of low voltages:

SCT−LV1   Every module shall have independent low voltage supplies.
               Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT−LV2   The low voltage levels shall be controlled to a precision better than 5% of
☒   maximum value at the module.
               Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV3   The analogue low voltage levels shall be known at the module to a precision
☒   better than 1% of maximum value.
               Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV4   The logical status of the low voltage supplies shall be monitored (see SCT−
☒   LV10).
               Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV5   Every Low Voltage power supply block supplying a number of detector modules
☒   shall have a connection to the hardwired interlock bus.
               Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV7   The resolution of the monitoring of the low voltages shall be better than 1% of the
               full range.
               Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV8   Overcurrent trip level for low voltage supplies shall be adjustable.
               Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT−LV9   The overcurrent limit should have a time setting.
               Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV10   The logical status of the low voltages should be reported as
☒   ON/OFF/TRIP/INTERLOCK/OVERTEMPERATURE.
               Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV11   At power 'switch−on' the crate controller shall be powered ready for
☑   communication and the output of the power blocks in the crates shall be switched
               off.
               Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−LV12   A temperature trip in Low Voltage power block shall interlock all the output
☑   channels in the block.

Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–LV13 The trips condition in a power block shall be readable by the crate controller.
☑   **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–LV14 Every power module shall have a bidirectional for sending out and receiving
☑?   interlocks.
           Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.2 Control and monitoring for high voltages:

SCT–HV1 Every module shall have independent high voltage supplies.
           Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV2 High voltage levels shall be controlled at the supply to a precision better than 5%
☒   of maximum value.
           Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV3 High voltage levels shall be monitored at the supply with a precision better than
☒   2% of maximum value.
           Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV4 Every High Voltage power supply block supplying a number of detector modules
☒   shall have a connection to the hardwired interlock bus.
           Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–HV6 The logical status of the high voltage supplies shall be monitored.
           Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV7 The current in the high voltage supplies should be monitored in multirange with
☒   highest precision (50nA) at low current and with 8 bit precission at high currents.
           Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–HV8 The high voltage supplies shall trip if the current exceed a preset value.
           Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV9 The current trip level for the high voltage supplies should be programmable by
           computer.
           Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–HV10 The ramp–up speed of the high voltage supplies should be programmable by
☒   computer with the range 5–40V/s.
           Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV11 The ramp down speed of the high voltage supplies shall be hard−wired giving a
☒   ramp down speed between 10s and 5s.
             Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV12 The logical status of the high voltages should be reported as
☒   ON/OFF/TRIP/INTERLOCK/OVERTEMPERATURE.
             Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV13 The maximum ramp−up step size shall not exceed 5V/s.
☑   **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV14 At power 'switch−on' the crate controller shall be powered ready for
☑   communication and the output of the power blocks in the crates shall be
             switched off.
             Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV15 A temperature trip in Low Voltage power block shall interlock all the output
☑   channels in the block.
             Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV16 The trips condition in a power block shall be readable by the crate controller.
☑   **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−HV17 Every power module shall have a bidirectional for sending out and receiving
☑?   interlocks.
             Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.3 Temperature monitoring

SCT−TMP1 The temperature shall be monitored on every module.
             Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT−TMP2 Temperature values shall be monitored inside SCT on every sector.
             Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−TMP3 The air temperature inside SCT shall be monitored for every section.
             Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−TMP4 The temperature in the cable bundle bringing power to the SCT inside the TRT
             should be monitored.
             Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−TMP5 The relative precision of the temperature measurement shall be better than 0.3 deg.

Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–TMP6 The absolute precision of the temperature measurement shall be better than 1   deg.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–TMP7 The temperature monitoring shall be functional after the power is cut in the
experiment.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–TMP8 The interlock signal generated by the temperature monitoring of a sector shall be
hardwired to the power supplies for the modules mounted on the stave generating
an interlock.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–TMP9 The trip temperature shall be individually adjustable for every sector.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–TMP10 The trip temperature should be hardwired and adjustable.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.4 Pressure monitoring

SCT–PRE1 The air pressure should be monitored inside the SCT.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–PRE2 The air pressure should be measured with a precision better than 1mbar.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–PRE3 The air pressure should be measured over a range from 960mbar – 1060mbar.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.5 Humidity monitoring

SCT–HUM1 The humidity should be measured inside the SCT for every section.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–HUM2 The humidity should be measured with a precision better than 1%.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–HUM3 The humidity should be measured over a range from 0% – 100%.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.6 Status monitoring

SCT–STA1 The status of the valves regulating the flow of coolant in the stave should be monitored for every section.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

4.7 General monitoring

SCT–GEN1 The monitored data should be normalized to 1 byte size by means of two scale ("zoom") linear conversion. The assumed number of gradations are: 128 – in both Normal and Warning substates, 64– in any Alarm and Fatal substates.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–GEN1 The monitored data should be normalised to 1 byte size by means of two scale ("zoom") linear conversion. The assumed number of gradations are: 128 – in both Normal and Warning substates, 64– in any Alarm and Fatal substates.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–GEN3 The radiation level inside the SCT should be monitored.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.8 Data logging

SCT–DAT1 All the information available from the control and monitoring shall be kept for minimum a week.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT–DAT2 The data from the control and monitoring shall be kept in compressed format after a week.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

4.9 Interfaces and links

SCT–LNK1 The Local Area Network (LAN) protocol should be used for inter–LCS
communications; it shall correspond to the standard DCS LAN protocol.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–LNK2 The 'Mini'–net protocol should be used for inter–node (inter–crate)
communications; it shall correspond to the standard DCS net–protocol.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–LNK3 The CAN–Open protocol should be used for inter–unit communications;
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

4.10 Interlocks

SCT–ILK2 Every High Voltage power supply block supplying a number of detector
modules shall have a connection to the hardwired interlock bus.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK5 The interlock signal generated by the temperature monitoring of a sector shall be
hardwired to the corresponding power supply block.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK6 The interlock generated by the radiation monitors, if any, shall be hardwired to all
the power supply crates.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK7 The configuration of the interlock, cross connection, should be known by
software.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK8 The interlock shall be filtered from fluctuations faster than 2 s.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK9 The reaction time for the hardwired interlock, cut time, shall be faster than 1 ms.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK10 The interlock signals shall be TTL levels with active=low and inactive=high
☑ **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT–ILK11 There shall be monitoring of radiation dose rate inside the Semiconductor Tracker.

☑   **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT−ILK12 The Semiconductor Tracker shall if necessary send a request signal to the LHC machine for a dump of the beam.

☑   **Need** essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

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1 ATLAS Detector Control System User Requirement Document, PSS05–ATLAS–DCS–URD, 15
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