Electrical Results from Prototype Modules

Abstract

This document describes the measured electrical readout performance of forward modules in the laboratory, in beam tests and in the SCT system test at CERN.

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Distribution List

History of Changes			
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1 Scope of the document.

The document summarises results on the electrical performance of forward modules read out with the ABCD3T version of the SCT binary ASICs [1,2]. In section 2 we list the the available modules that have been studied, section 3 describes the tests we performed and their motivation., sections 4 to 7 show the results on the performance of the modules and, finally, section 8 summarises the results obtained.

2 Performance goals of the modules.

The end-cap module electrical specifications are described in [3]. In brief, the modules need to fulfill the following conditions:

- Signal over noise ratio of about 14:1 before irradiation, reducing to about 12:1 after 10 years of operation.
- Noise occupancy < 5×10^{-4} which means that the operational threshold needs to be set at 3.3 times the average RMS of the noise.
- Tracking efficiency > 99%.
- Capability to tag beam crossings.

These requirements translate into requirements on the module electrical stability, the noise -to ensure the proper noise occupancy level and signal over noise ratio-, proper matching of the channel discriminator and front-end rise-time.

3 Available electrical modules.

In order to ascertain the electrical performance of the ATLAS SCT forward modules, a number of them have been built. Table 1 list them all, specifying which tests have been carried out on the different modules.

Module	***Type***	***Hybrid type***	***Irradiated***	***Data***			***Cal. factor***
				Lab. tests	***Test beam***	***System test.***	
K5-300	Middle	CICOREL		✓		✓	1.093
K5-301	Middle	CICOREL		✓	✓	✓	1.093
K5-302	Outer	CICOREL		✓	✓	✓	1.150
K5-303	Outer	CICOREL		✓		✓	1.171
K5-305	Outer	CICOREL	✓	✓	✓		1.171
K5-308	Outer	CICOREL	✓	✓	✓		1.095
K5-309	Outer	CICOREL		✓			???
K5-310	Outer	CICOREL		✓	✓		1.095
K5-312	Outer	CICOREL		✓	✓		???
K5-400	Outer	DYCONNEX		✓		✓	1.171
K5-402	Outer	DYCONNEX		✓		✓	1.171
K5-304	Inner	CICOREL		✓	✓		1.171
K5-307	Inner	CICOREL		✓			1.150
K5-313	Inner	CICOREL		✓			1.095
K5-314	Inner	CICOREL		✓			1.150
K5-316	Inner	CICOREL		✓			1.150

Table 1. SCT Forward electrical modules

In all the measurements the ASICs are powered with the prototype SCT low voltage power supply, SCTLV3, and readout electrically via an SCT CLOAC-MuSTARD-SLOG system [4]. The sensors are biased with the companion prototype high voltage units (SCTHV).

The amplitude of the calibration pulse issued by the ASICs needs a correction factor that takes into account variations from the design value of the calibration capacitor on the front-end. These values are also compiled in Table 1.

Three of the modules have been irradiated with the 24 GeV proton beam of the CERN PS using the SCT irradiation facility [5]. The modules have been irradiated up to a fluence of 3×10^{14} protons/cm^2.

4 Results from individual modules.

The characterization of a single module has to demonstrate its functionality and that the performance of the ASICs does not degrade when assembled into the module. To this end, front-end parameters, like the gain, output noise, offset spread and timewalk need to be measured and it should be verified that their values are uniform across single chips, as specified for the ASICs. Additional test made using a source setup will determine the signal over noise ratio.

4.1 Gain, noise and noise occupancy.

For unirradiated modules, the measurements have been made with a temperature on the hybrid of about 35ºC. At this temperature the noise in all the modules stays in the range between XXX and YYY e^- ENC as illustrated in Figure 1 where the average equivalent noise charge, in electrons, is shown for each of the 12 ASICs in all the modules tested.

Figure 1. Measured noise (e^- ENC) on each of the 12 ASICs of all the modules tested. The temperature of the hybrid was measured to be about 35ºC.

Figure 2 shows a similar plot for the average gain spread on each of the 12 ASICs of the modules. The gain variation in the chips is of the order XXX% and therefore its contribution to the noise is negligible. The average module gain is XXX mV/fC.

Figure 2. (a) Average gain spread on each of the 12 ASICs of the modules.(b) Average gain on each of the 12 ASICs of the modules.

In the ATLAS operating conditions the temperature on the hybrid will be of about XxºC. Since the noise of the ASICs decreases with temperature with a slope between 5-10 e- ENC/ºC [10], the noise will be about XXX electrons smaller than the one measured at 35ºC. At this temperature the signal over noise ratio is already XXXX, thus satisfying the preirradiation performance goal. Measurements made with a source setup and on the beam test confirm this value.

Figure 3. Noise occupancy as measured on a single link on an unirradiated module.

The SCT design goal is to set the ASICs single strip binary readout threshold at 1 fC, to ensure the high tracking efficiency for particles traversing the silicon at inclined angles, depositing charge on more than one readout strip. It is therefore important that the threshold value is greater than 3.3 times the average rms of the noise to achieve the noise occupancy required. In non irradiated modules the mean noise occupancy is ~10^{-5}, well below the requirements. Figure 3 shows the mean noise occupancy of one side of a module.

Figure 4. Noise occupancy as measured on a single link on an irradiated module.

The three irradiated modules have been measured with temperatures on the hybrid around 0ºC. For those modules the average ASIC's noise is about XXXX e^- ENC. The noise occupancy at 1 fC threshold is XXXX.

4.2 Threshold uniformity.

For the binary architecture, one of the most critical issues is the uniformity of parameters of the front-end circuit and, specially, matching of the discriminator threshold. The ABCD3T chip ensures that by the implementation of individual threshold correction in every channel using a 4-bit DAC (trim DAC) per channel with four selectable ranges.

Figure 5. Offset spread on each of the 12 ASICs in an unirradiated module.

Figure 5 shows the offset spread on each of the 12 chips of an unirradiated module after trimming the threshold for all the channels. As can be seen, the average value is about XXX mV (or ~XXX fC). This is to be compared with the noise value of XXX fC.

Figure 6. Offset spread on each of the 12 ASICs in an irradiated module.

For the irradiated modules the matching of the discriminators degrades and, therefore, a wider range of the trim dac is needed to reduce the offset spread, see Figure 6

4.3 Timewalk.

In order to ensure a proper beam crossing identification and to reduce the inefficiency produced by the assignment of hits to the wrong time slot, the timewalk should be smaller than 16 ns [1,2]. Here the timewalk is defined as the maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC.

Figure 7. Timewalk for unirradiated modules..

Figure 7 shows the measured average timewalk on each of the 12 ASICs of the non-irradiated modules. Figure 8 shows the same quantity for the irradiated modules.

Figure 8. Timewalk for irradiated modules..

4.4 BER testing of opto-links.

Here ?

4.5 Source setup.

5 System test and first results.

5.1 General Description

The goal of the system test is to run as many modules as possible in a physical configuration which is as close as possible to the planned ATLAS SCT configuration, thereby testing the performance of the modules in such a system and comparing it to their stand-alone performance. Experiments are performed to ascertain the robustness of the grounding and shielding schemes used against extra noise pick-up from the experimental environment.

The system test simulates a section of one of the SCT forward disks in all its details of mounting, cooling, supply and shielding. Details on the sector prototype can be found in [6].

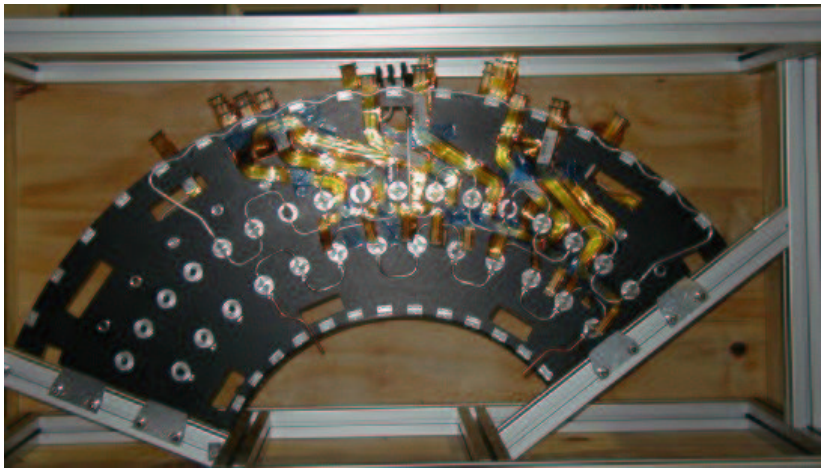

Figure 9. Sector Front view.

The sector can accommodate up to 33 modules; 13 outer, 10 inner and 10 middle modules. Figure 9 shows the outer and inner module mounting positions on the front of the disk, while figure 10 is of the back of the disk where the middle modules are mounted. The mounting positions are denoted O1-O13 for outer and I1-I10 for inner positions starting at the far left of figure 9. While the middle position are denoted M1-M10, counting from the right of figure 10.

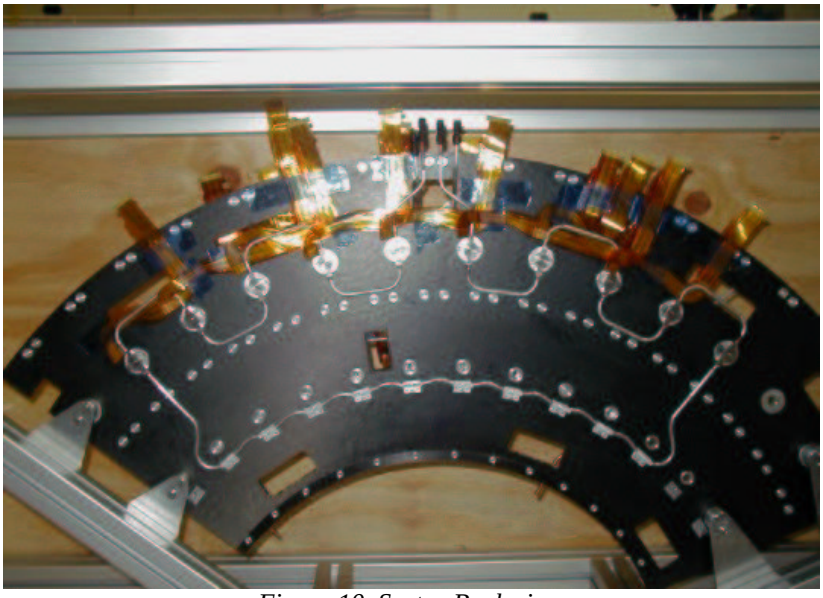

Figure 10. Sector Back view

The disk is held at each end via metal bolts to an aluminium support frame, shown in figures 9 and 10. The carbon-fibre disk is therefore in electrical contact with the support frame. The sector is housed in a copper box to represent the thermal shield at the SCT. It should be noted that the cover is not electrically or geometrically similar to the planned ATLAS SCT thermal shield. Combined with blackout cloth and a dry nitrogen supply the copper box provides a dry and dark atmosphere, with a relative humidity of 20% or less, whilst running.

Separate cooling circuits are used for the three module types. The inner modules are served via a CuNi pipe 4mm OD with 70µm wall thickness, while the middle and outer modules have aluminium pipes 3.6mm ID/ 4.0mm OD. The cooling blocks are machined Al blocks with copper plating at the pipe block join. The block was soft soldered to the cooling pipe. On the outer cooling circuit 4 of the high cooling blocks are CC with a Cu plate (positions 3,5,7, and 9 counting from the left as you look at the disk). The third CC block had a final gold flash to prevent oxidation. An ethanol-water mixture is pumped through the pipes with the temperature being controlled by a commercial chiller.

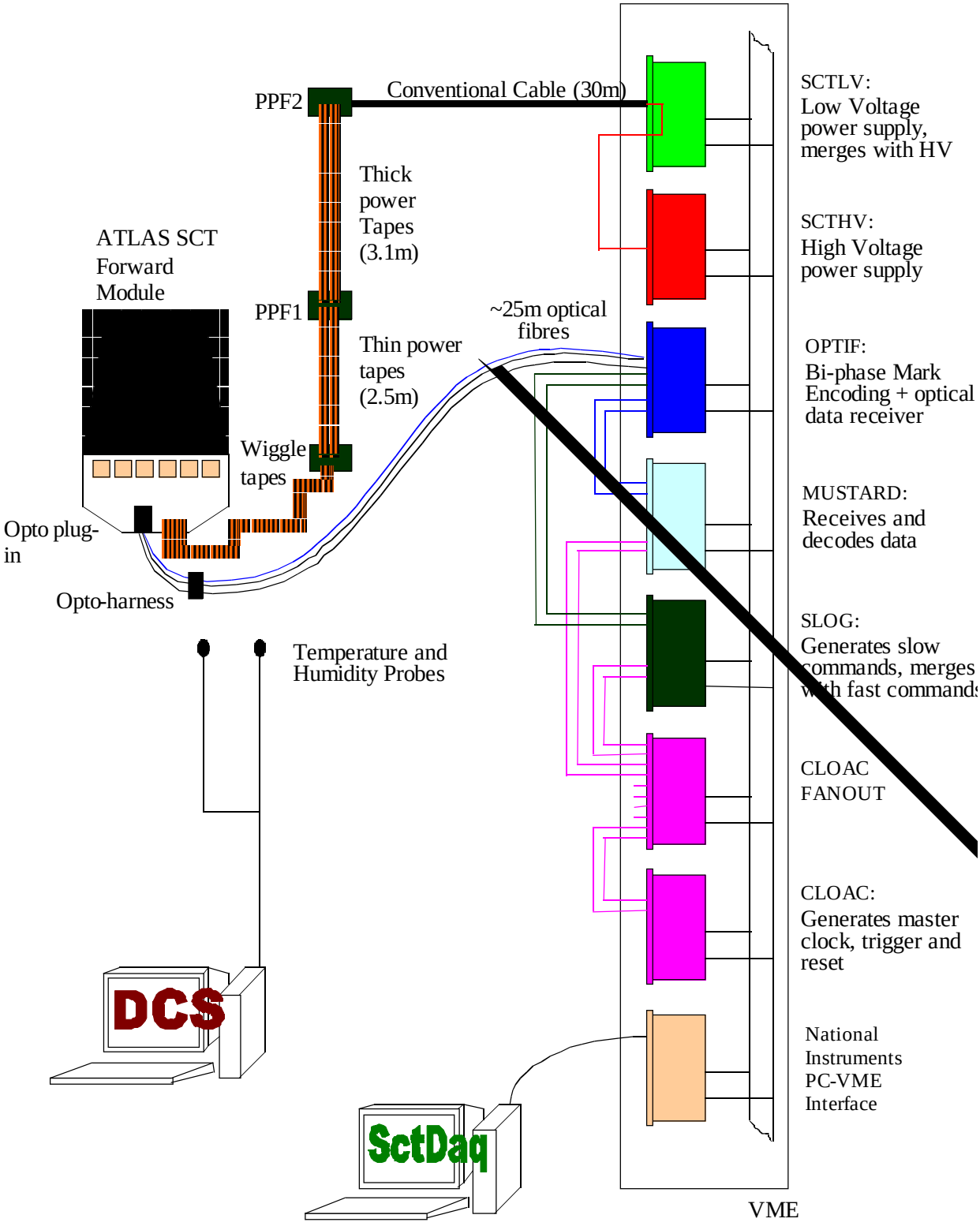

Figure 11. A schematic layout of the forward SCT system test.

The low mass wiggly power tapes were produced at Ljubljana. They were made from the ‘old’ design being ??mm wide with Al tracks. Because of the expense of producing different shapes of tape, only 9 different designs were produced. Therefore 9 positions have the correct tape layout and the remaining positions have tapes which have

been ‘made to fit’ as best as possible. The wiggle tapes contain all the power, select, reset and temperature monitor lines for the modules. The communication of data to and from the module is performed via the optical plug-ins in the forward optical harness. Each harness serves either 5 or 6 modules. At the edge of the disk the harness connects to 25 m long fibres, which transmits the data to the DAQ system, illustrated in Figure 11.

The SCT prototype VME power supplies (SCTLV3s) power the module's ASICs and opto-components. The detectors are biased with the companion prototype high voltage units (SCTHVs). The individual channels of each power supply are floating with respect to each other. It should be noted that the return lines of the ASIC analogue and digital lines and the detector bias line are connected together at the disk in a fashion dependent on the particular grounding and shielding scheme implemented, which are described later.

The modules are read out using a CLOAC-SLOG-MuSTARD-OPTIF system, with the OPTIF [4] providing the electrical-optical interface. The DAQ used is in place of the final read-out drivers, (ROD). The hybrid temperature is readout via the SCTLV3 modules. A ROOT-based SCTDAQ software package is used, running on a Windows-NT PC connected to the VME crates via a National Instruments interface card.

Control and monitoring of all voltages and currents is carried out through the DAQ software, although a prototype DCS system is used to monitor hybrid temperature, environmental temperature and humidity and control the cooling unit.

All patch panels and power tapes used are as close as possible to the planned final ATLAS design, except for extra provisions on the patch panels to allow testing of various coupling schemes. From the power supplies 30 m long conventional cables run to PPF2 via a common mode choke. These chokes are intended for use at PPF3 but PPF3 is not represented in the system test. Between PPF2 and PPF1 2.5 m long kapton tapes with 100µm thick Al tracks are used. The kapton tapes between PPF1 and PPF0 are 3.1m long with 50µm thick Al tracks. A schematic diagram of the system test is shown in Figure 11.

5.2 Grounding and Shielding in the System Test

The system test bases it's grounding and shielding scheme on the proposal outlined in [7,8,9]. The main elements as applied in the system test are described below, with any differences noted. Two grounding and shielding schemes are being investigated. They differ in the way the modules are referenced with respect to each other.

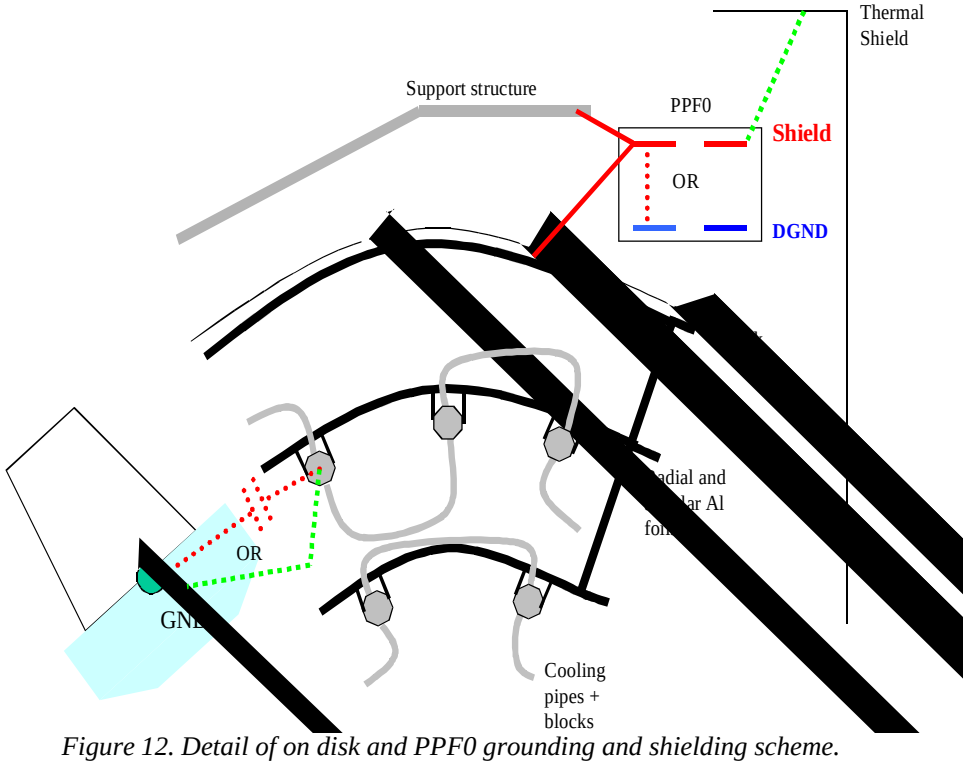

Figure 12. Detail of on disk and PPF0 grounding and shielding scheme.

The conventional cables are shielded and this shield is commoned through the chokes to the kapton tapes side. From PPF2 to PPF1 the 6 “thick” kapton tapes per PPF2 are bundled together and wrapped with aluminium foil. At PPF2 the shield is connected, via jumpers, to the aluminium foil wrapped around the kapton tapes and taken to

PPF1. PPF1 is electrically shielded inside an aluminium box, connected to the kapton aluminium foil shield. PPF1 is equipped with jumpers to allow AC connections (with 2.7 µF) between VDD and VCC to the cable shielding. These jumpers have been present for all tests so far. From PPF1 to PPF0 the "thin" kapton tapes are bundled together in sets of 3, with each set wrapped in aluminium foil. The shield connection continues via the aluminium foil around the "thin" kapton tapes to the sector housing. The shield is held in good contact with the copper box.

The disk's aluminium support structure, inside the copper box, is electrically connected to the support structure via copper tape and via supporting screws into the structure of the disk.

The kapton tape bundles split on entering the copper box on route to PPF0 while the aluminium foil wrapper stops at the copper box. For both grounding schemes the shield of PPF0 is connected to a 50µm thick angular aluminium foil stuck to the outer edge of both faces of the disk. The foils are connected together and to the carbon fibre of the disk with conductive epoxy and copper tape. On each disk face the angular foil is connected via three radial foils to angular foils running just above the cooling blocks, (2 foils on the disk front and 1 on the back), with foil tabs down to each cooling block. Connections are made between the foil and the cooling block using either conductive epoxy or the cooling block's fixing screws. In this manner all the cooling blocks are connected, via the aluminium foil, to the outer angular foil and thus the shield of PPF0. The shield at PPF0 is also connected to the aluminium support structure via short pieces of copper tape. The detail of the on-disk-grounding scheme is shown in Figure 12.

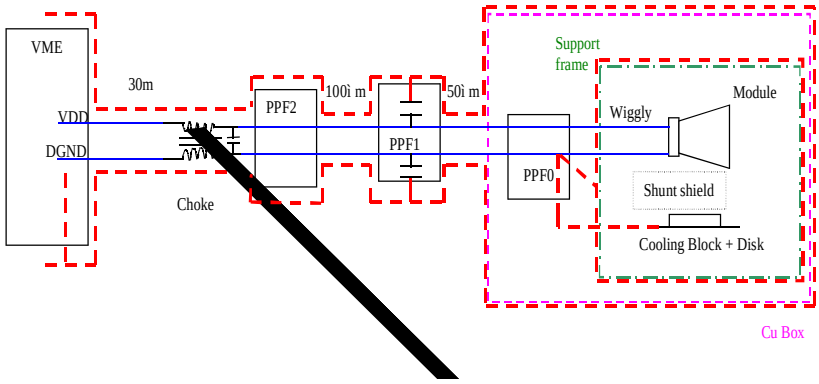

Figure 13. Grounding and shielding scheme that utilises the shunt shield

The first grounding & shielding scheme to be investigated prescribes the control of stray capacitance between the cooling pipe and the silicon detector backplane by the use of a shunt shield placed between the module and the cooling block. The shunt shield is an integral part of the K5 module consisting of a copper foil at the cooling point of the module connected directly to Analogue Ground, (AGND), of the module. Electrically insulating foam with good thermal properties is mounted onto the cooling block face to insulate the module from the cooling block. Therefore the module ground and the cooling block are not in intimate electrical contact with each other. For this grounding scheme the shield connection at PPF0 is connected to Digital Ground, via jumpers fitted to PPF0. Thus the cooling circuit is connected to the modules digital return. At the SCT low voltage power supply the conventional cable shield is directly connected to Digital return of the power supply. Figure 13 illustrates the main features of this grounding scheme.

The second scheme requires the module grounds to be held together as tightly as possible. The module shunt shield is shorted so that the module power returns are DC connected to the cooling block at the module mounting point. The electrically insulating foam remains on the face of the cooling block. To have a direct connection from the module grounds to the block an additional metal covered kapton washer, connected to AGND of the module at the module connector, is glued onto the top of the module's peek washer. The metal holding nut on the cooling block insures a DC connection between the module power returns and the cooling block. At PPF0 the shield is connected to an aluminium foil that is routed with the "thin" kapton tape between PPF0 and the copper box. The low voltage power supply has shield connected via a 10nF capacitor to VME ground. The main features of this scheme are shown in Figure 14.

In figures 13 and 14 the red dotted line represents the shield, only VDD and DGND lines are shown but in reality both analogue and digital lines pass through a choke and are decoupled to the shield at PPF1.

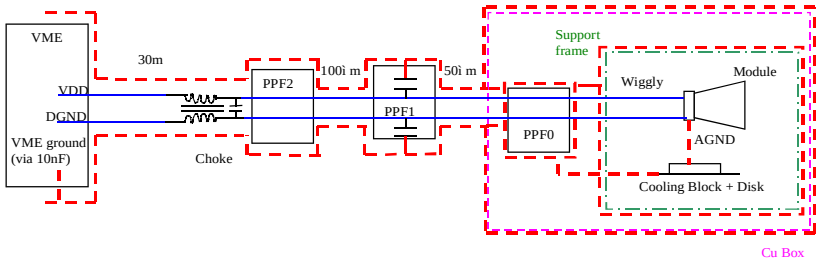

Figure 14. Grounding and shielding scheme that utilises DC coupling between the AGND of each module

5.3 *First results for the Forward system test.*

When a module arrives at the system test, it is accompanied by the results from a standard characterisation as performed at the module building cluster. The first step in integrating the module into the system test is to repeat this standard characterisation on the 'electrical test bench' in the system test lab, to verify that the module has not suffered in transit. The electrical test bench is considerably simpler than the full system test as it bypasses the optical communication, and uses only very short power and signal cables. Therefore a module may be expected to give its best performance when running stand-alone 'on the bench'.

Once the module is verified to be in good working order, it is mounted on the system test sector (with all grounding and shielding connections made), and the standard characterisation sequence is repeated, powering only that one module. This performance is compared to that on the bench and any differences are noted and investigated if possible. When this comparison is complete, the module is considered ready to be included in multi-module tests.

Once the module is verified to be in good working order, it is mounted on the system test sector (with all grounding and shielding connections made), and the standard characterisation sequence is repeated, powering only that one module. This performance is compared to that on the bench and any differences are noted and investigated if possible. When this comparison is complete, the module is considered ready to be included in multi-module tests.

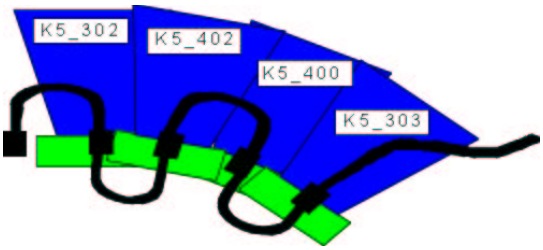

Figure 15. modules & cooling pipes in a 4 outer multi-module run

There are currently six modules (two middle and four outer modules) in the system test, detailed in Table 1. All the modules showed approximately the same noise values (within about 100 ENC) when running alone on the sector as they did on the bench.

A typical multi-module test is to measure the gain and noise with many modules running in parallel. This has been performed, using a three-point gain calculation and noise occupancy scans, with the modules on the sector. Detailed multi-module studies have only been performed with the shunt-shielded grounding scheme implemented. At present either the two middle modules or the four outer modules have been operated together, but not all six at once. For example the 4 outer modules were mounted in positions O10 to O13 (O11 and O13 being high blocks) as shown in figure 7. The modules were communicated with via a single opto-harness. Details are given in table 2.

Module	*Cooling block*	*Opto plug-in*	*Temperature (C)*
K5-302	O10	3	34
K5-402	O11	4	37
K5-400	O12	5	35
K5-303	O13	6 (only link1 working)	37

Table 2. Multimodule tests on 4 outer modules.

The measured noise values of all ASICs on the modules, with all 4 modules in operation at a hybrid temperature of about 36^0C, are shown in Figure 5. With the exception of the first chip on module K5-303 the noise values lie in the anticipated range.

No 'dead seagulls' were seen in the distribution of noise across the modules when operated on the sector. Such 'dead seagull' noise distributions were seen previously and attributed to correlated noise sources.

A scan of Noise occupancy as a function of threshold, in charge, was performed. Good agreement in noise between the 3point gain and the Noise Occupancy runs were obtained.

(comment of level of NO wrt design requirements)

Noise occupancy as a function of time was measured with the threshold set to 1fC on all modules. The duration of a noise occupancy measurement was about 1 minute, with a 2 minute interval been measurements. 100 measurements were made. A decrease in noise was observed as a function of time, this was also seen in the barrel system test. There are no peaks detected in the noise occupancy as a function of time plots. Had peaks been present (also observed in the barrel due to the pick-up by the system of the switching currents of the air-conditioning) this would be indicative of inadequate shielding.
The Correlated noise data taking macro has been run for the 4 modules. The noise calculated from the correlated noise measurement agreed with those from the 3pt gain scan, while the amount of correlated noise found was low and consistent with zero.

Detailed multi-module runs have not at present been performed with the common grounding scheme.

Figure 5 - ENC from 3point gain

5.4 Noise injection studies with shunt shield grounding option

6 Module Test-Beam results.

6.1 Introduction.

Testbeam measurements have been performed to evaluate the tracking performance of a number of the SCT end-cap modules prepared for the module FDR. The measurement program was designed to investigate the response of individual modules to single high-energy particle tracks through a range of systematically varied operational and environmental parameters. These results may then be used to study the expected performance in ATLAS at much higher trigger rates and track densities. Two of the modules tested were those irradiated previously at the CERN PS T7 facility to the SCT reference dose of 3×10^{14} p/cm^2. Related beamtests have been performed in previous years on barrel SCT modules (which have much in common with SCT barrel modules, including basic detector technology and the same readout ASICs)[2,3], and prototype end-cap modules [2].

6.2 Facilities and setup.

The beamtests were performed at the ATLAS testbeam facility at the CERN SPS H8 beamline. A collimated, parallel beam of 180 GeV/c pions with some muons, about 1cm across, travelling in air, is passed through a pair of trigger scintillators and an inline array of silicon detectors as shown in figure 1. The particle type and energy is chosen to provide minimal multiple scattering within the SCT setup while allowing adequate beam intensity. Beam intensity is set to around 20,000 particles per second for the duration of the SPS spill, 4.8 seconds in a 16.8 second cycle. Up to 10 SCT modules under test are arranged one after the other, presenting approximately the same aspect to the incident beam. The modules are mounted on a rack which rotates each module about its own axis through a range of about +/- 15° from normal, the whole array being always at the same angle to the beam. Each SCT module is contained in its own module box of a standard design incorporating liquid cooling to the module design cooling surfaces. The boxes are enclosed in perspex cover sheets to present minimal material to the beam while enclosing each module in its own thermal environment. These ten modules and their associated mechanics are all contained within a larger thermal enclosure flushed with cold nitrogen gas. The liquid coolant and the gas are maintained between -10 and -20° C in order to keep the module temperatures close to their design operating temperature of around -10° C.

A major feature the ATLAS H8 facility is a large superconducting dipole magnet. The SCT setup sits on a carriage which can be inserted into the field of this magnet. The field is set to 1.56 T when used, is approximately uniform, and is directed vertically downwards. This allows modules to be arranged with their strips parallel to the field direction while facing the beam at normal incidence, a configuration which mimics that of the barrel modules in ATLAS and which has been studied extensively in previous beamtests to investigate effects of the Lorentz force. End-cap modules in ATLAS will be arranged with their strips radiating away from the axis at right angles to the

nominal solendoidal field direction. This configuration is not available at H8. However, since the electric and magnetic fields are parallel and the effects of the field on charge collection times or distributions are not expected to be large, relatively few measurements with the magnetic field in accessible configurations were done.

In addition to the 10 SCT modules, the SCT testbeam facility is equipped with four X-Y pairs of tracking detectors forming a silicon telescope. These are arranged in pairs immediately upstream and downstream of the thermal enclosure. Their function is to provide high spatial resolution space points from which independent, high resolution tracks through the modules under test can be reconstructed. They utilise 50 μm pitch silicon detectors with analogue readout ASICs which, with charge division, allow tracks to be reconstructed to around 3 μm resolution at the modules under test. The readout ASICs are VA2, with around 1 μs shaping and 10 ms multiplexed readout time. Use of these non-pipelined chips limits both the trigger rate (due to the readout deadtime) and the beam intensity (due to track identification and pileup).

An important characteristic of the SCT readout ASIC, the ABCD3TA, is the short shaping time of 25 ns coupled with the clock-synchronous nature of the comparator sampling. Precise timing is therefore required in order to measure in detail the pulse shape and to determine the optimum timing settings as functions particularly of radiation damage and magnetic field. As the SPS fixed target beam is not clock-synchronous, the signals in the SCT readout chips are random in time with respect to their clock. The beamtest is therefore equipped with a 0.2 ns resolution TDC and an SCT CLOAC trigger synchronisation module. The CLOAC delays propagation of external triggers both for the integer number of clock cycles required for the pipeline and for the fraction of a clock cycle required to synchronise the trigger with the internal sampling. This fractional clock delay is measured by the TDC allowing offline selection of timing windows from the initial random data set.

Data acquisition uses the standard SCTDAQ setup, including the SLOG, MuSTARD and CLOAC SCT VME modules and the ROOT software package, extended to readout the telescope and TDC. Modules are electrically connected to the readout system using their spy connectors rather than optical readout. Low and high voltage power supplies are also the standard SCT VME modules.

[figure 1 : beamline sketch for 2002.]

6.3 Measurement goals and program.

The basic testbeam measurement of SCT binary modules is a scan of the input comparator thresholds resulting in s-curves of particle detection efficiency versus threshold. Several tens of thousands of randomly timed events are taken a each threshold point. Each event is analysed for matching telescope tracks and optimal timing efficiency to determine an efficiency. From these data, the efficiency around the design operating threshold, 1.0 fC, can be determined, as can the mean charge response, the threshold at 50% efficiency. Measurement of the mean charge response allows an absolute calibration of the internal charge injection calibration circuits of the readout chips. By studying the same data as a function of timing window cuts, the pulse shape can also be mapped. Combining the mean charge response with measures of the noise allows signal-to-noise ratios to be determined. Combining the experimentally determined charge scale with separate noise measurements allows a determination of the expected noise occupancy at operating thresholds along with a measure of the operating margin. Analysis of a large number of events at the operating threshold also allows a determination of the spatial resolution and mean cluster size.

The set of modules included in the beamtest was largely determined by the availability of the two irradiated Outer modules, #id and #id. Two unirradiated Outer modules, #id and #id, were therefore also included for direct comparison. Two Inner/Middle (???) modules were also included, as were two previously measured barrel modules as reference samples. [Any mention of the KBs ??]

The first goal of the beamtest program was the measurement of these important module parameters for a minimum ionising particles at normal incidence to the silicon planes. This configuration is the reference configuration for comparison with other beamtests and for parametrising the basic module performance. The detectors were biased at their design operating voltages, measured at the high voltage supplies, of +150V for the unirradiated modules and +400V for the modules that had been irradiated at the PS to the SCT reference fluence, representing the extremes of radiation history. A greater number of events than standard were taken for this basic scan to provide higher statistics for timing window and spatial resolution studies.

A second goal was the measurement of the bias voltage dependence of the modules, especially the irradiated modules, since this is important operational information. This measurement consists of repeated threshold scans at several bias voltages from which the shape of the mean charge versus bias curve can be determined.

A third goal was the measurement of the performance at various angles of rotation about an axis parallel to the central strips of the module. Threshold scans at nominal bias voltages at different angles were performed up to the maximum accessible at H8. From each scan, the dependence of the efficiency at operating thresold and the mean cluster size versus bias can be determined.

A fourth goal was a mapping of the position dependence of the module performance. This was performed at normal incidence by taking threshold scans at several positions around the silicon sensitive area. This included positions near and far from the end-tap electronics hybrid position, to study effects of the distance from the readout amplifiers as well as of the varying strip pitch, as well as several positions across the module.

A last measurement was several threshold scans with the magnet on, at 1.56T at several angles, and at nominal bias, primarily to confirm the expectations from the previous barrel measurements.

6.4 Results.

[Sets of figures similar to the Barrel FDR]

Table ? lists the modules tested with a summary of the important resulting parameters.

7 Summary.

Summary of results.

8 References

[1] ABCD3T specifications.

[2] W. Dabrowski et al. *Progress in Development of the Readout Chip for the ATLAS Semiconductor Tracker*. Proceedings of the Sixth Workshop on Electronics for the LHC Experiments (LEB2000), Krakow, September 2002.

[3] Electrical Specifications and Expected Performance of the End-cap Module, ATL-IS-EN-0008.

[4] http://sct.home.cern.ch/sct/sctdaq.html

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[11]