ATL-IS-EN-0007

Thermal and Mechanical Specifications and Expected Performance of the Forward SCT Module

Steve Snow. Version of 15/7/02

Abstract

This document defines the module thermal and mechanical specifications and explains why they are necessary. It also reports on those features of the thermal performance which can be calculated directly from the design.

Contents

1 Summary of Requirements

The **dimensional** specifications for the forward SCT module are derived from the following considerations:

- The need for the modules to fit in to the places designed for them on the disks without mechanical or electrical clashes.
- The need to make a good thermal contact between the module and the cooling/mounting block, which sets requirements for the planarity and parallelism of the contact surfaces.
- The need for the amount of overlap in the sensitive area between adjacent modules to be sufficiently large to allow alignment with tracks on a reasonable timescale.
- The need for the relative position of the four detectors that make up a module to be sufficiently close to the design position that we can treat all modules as being identical in track finding and fitting. Re-fitting with individual treatment of module geometry should only be necessary for the very highest precision physics.

The **thermal** specifications are derived from the following considerations:

- The need to remove the maximum power that can be generated by the front-end chips while keeping them sufficiently cool to avoid excessive thermal noise.
- The need to remove the maximum power that can be generated by leakage currents in the detectors, plus any power picked up by convection and radiation from the environment, while keeping them sufficiently cool. The acceptable detector temperature is chosen to avoid thermal runaway, to allow beneficial annealing of radiation damage and to prevent high leakage currents which generate extra noise.

The **thermo-mechanical** requirements are that the module must be able to withstand both the thermal gradients that it will experience under the highest expected power loads, and the many temperature cycles between the highest and lowest temperatures that it may be subjected to. Any permanent distortion of the module which is caused by these thermal conditions must be small compared with the dimensional tolerances. Any distortion of the module between room temperature and operating temperature must be repeatable and module-to-module differences in distortion must be small compared with the dimensional tolerances.

The requirements on the module **mechanical strength** are that there must be a negligible risk of breaking the module while assembling, testing and mounting or removing it from the disk.

The thermal and mechanical properties of the module must not be significantly affected by the radiation dose that we expect it to receive.

Finally, the module should meet all of these requirements while having the lowest possible percentage of a **radiation length**. We expect this minimal value, averaged over the sensitive area of 12 cm modules, to be less than 1.3 % X_0.

2 Detailed Specifications

1. We require a clearance of at least 1 mm between the closest points on any two modules when they are mounted on the disk. The same clearance is required between a module and any other object such as the cooling, power tapes or support structures. This is required to avoid clashes during module mounting and to be safe against potential differences of up to 500 V. The clearance around a module is determined by the module support structure which is not yet finalised. The task of this document is to define the module envelope, which is detailed in Section 3.
2. The module mounting/cooling surfaces must lie in a single plane to an accuracy of better than ± 30 microns. A similar specification applies to the surface of the blocks and ensures that the thickness of the thermal grease interface will be less than 30 microns when averaged over the surface area.

3. The placement of the four detectors relative to each other and relative to the module mounting points is specified in detail in [6] and a summary is given in Section 4 of this document. Our target can be outlined as: Wafer-to-wafer in plane; 5 microns transverse to strips, 10 microns along strips. Four-wafer assembly to mounting points in plane; 20 microns. Wafer surfaces to mounting surface perpendicular to plane; 115 microns.

4. We take the maximum normal power consumption of the hybrid to be 6.8 W and the maximum possible power to be 8.8 W. An upper limit on the power consumption of the detectors, after 10 years of irradiation and when biassed to 460 V, is taken to be 185 W/m^2 at 0 C. We must add to this an upper limit on the combined convection and radiation heat load on detectors which is 0.2 W per detector. So we define the **maximum load** condition as a hybrid power of 7 W and a detector power of 185 W/m^2 at 0 C + 0.2 W per detector. These power values are explained in Sections 5 and 6. There is a shallow optimum in the balance between harmful and beneficial annealing effects at around -7 C. Furthermore, at temperatures above -7 C the increased leakage current of an irradiated detector will start to make a significant contribution to the noise [7]. Therefore we specify that at maximum load the detector must be cooler than -7 C.

5. There is also thermal runaway to consider. Since this is a hard failure unlike the previous example, we add a 30 % safety factor to the electrical power to get 240 W/m^2 at 0 C + 0.2 W per detector and call this the **overload** condition. We specify that when subjected to the overload condition the module must not go into thermal runaway.

6. The extremes of temperature which the module must be able to survive while unpowered are taken to be -30 to $+50$ C. In addition it must be able to survive the temperature gradients caused by operation at maximum power with all the power taken out through the cooling points. These gradients must be survived at both ATLAS temperature (cooling block at -20 C) or lab testing temperature (cooling block at $+20$ C). By "survive" we mean that any permanent deformation of the module dimensions must be less than 50% of the asssembly tolerances.

7. When a module is taken from room temperature (where it is surveyed) to operating temperature and powered it will certainly shrink and possibly distort in some other way. Provided these distortions are repeatable from module to module we can correct for them. Therefore we specify that the distortion is repeatable at a level of less than 50% of the asssembly tolerances.

8. The forces exerted on a module when connectors are (un)plugged in to it and when it is (un)mounted on a disk are described in [4]. We specify that the module must not be damaged by these or other normal handling forces.

9. After a radiation dose of 3×10^{14} protons/cm^2 the module must not show any sign of damage to its mechanical or thermal properties.

10. The Inner Detector TDR specified the radiation length of the outer and middle ring modules, averaged over the sensitive area of the detectors, to be $1.28\% X_0$. We should not exceed this value in the final design.

3 Module envelope

The module envelope in-plane is sufficiently well defined by the drawings [1].

The envelope in the out-of-plane direction needs some more detail. There are two parts to the module; the hybrid area which has larger thickness with larger tolerances and the detectors area which is thinner and flatter. Within the hybrid area there is a region on the front side near the wrap-around where modules do not overlap each other; the thickest components are concentrated here and they exceed the envelope described below, see [3] for details. The fan-ins area is intermediate in thickness and will fit inside the same envelope as the hybrid. We define our reference plane as being the surface of a pair of ideal cooling blocks which are perfectly flat and parallel with each other. When a module is mounted on these blocks nothing in the main part of hybrid area will extend more than 2.5 mm

Component	Nominal thickness	Tolerance	Cumulative upwards	Cumulative downwards
C-C substrate	500	± 50	+550	0
Glue foil	75	± 5	+630	-80
Cu/Kapton flex	330	± 40	+1000	-450
Chip glue	50	± 30	+1080	-530
Chip	500	± 20	+1600	-1050
Wirebonds	300	± 300	+2200	-1650
Hybrid bowing	0	$+300/-200$	+2500	-1850

Table 1: Out-of-plane envelope of the hybrid area (microns).

Parameter	Tolerance	Effect on σ_ϕ (μm)
mhx,mhy,msy	20 μm	n/a
msx	100 μm	n/a
sepf,sepb	10 μm	0.0
midxf	10 μm	0.0
midyf	5 μm	2.88
a1 - a4	0.13 mrad	1.30
stereo	0.13 mrad	2.62
Sum in quadrature		4.10

Table 2: Tolerances of module geometry parameters and their influence on the ϕ resolution of space points.

above or 1.85 mm below the reference plane. The build up of tolerances which define this envelope are shown in Table 1.

The detector area is built to a pre-defined thickness which is independent of its components. Variation of the component thicknesses within their tolerance is taken up by the glue layers. The top surface of the detectors is specified to be at $+875 \pm 115$ microns and the lower surface of the detectors is specified to be at -375 ± 115 microns from the reference plane. These numbers are based on a spine thickness of 500 microns, glue thickness of 90 microns and detector thickness of 285 microns. In addition, specification 7 allows the possibility that the detector area may show a reversible deflection on cooling from room temperature to operating temperature of up to ± 57 microns. Then there are the detector-to-detector wire bonds which can be up to 600 microns high. So the envelope of the detector area above the reference plane is $875 + 115 + 57 + 600 = 1647$ microns. In the downwards direction it is $375 + 115 + 57 + 600 = 1147$ microns.

4 Detector Alignment

The procedure used to set the space point alignment specifications is described in this paragraph. It is inevitably a bit arbitrary but the reasoning goes as follows. We used a simulation program to measure the accuracy with which tracks could be reconstructed in the inner detector, assuming that the only uncertainty was that due to the intrinsic resolution of the detectors. This can be called the ideal inner detector performance. We then found a set of space point alignment errors which would have the effect of degrading the inner detector performance by no more than 20% from its ideal value, where 20% is just an arbitrary small number. These misalignments were chosen randomly for each module and they were applied to all subdetectors of the inner detector. The rule was that their combined effect must be less than 20% on each of the track parameters. It was usually the case that impact parameter and transverse momentum resolution end up setting the alignment specs, but in a few cases rapidity resolution is the limiting factor. The result of this study was that space point alignment r.m.s. accuracies of 12 microns in the ϕ direction, 50 microns in the R direction and 200 microns in the z direction were chosen for the forward SCT.

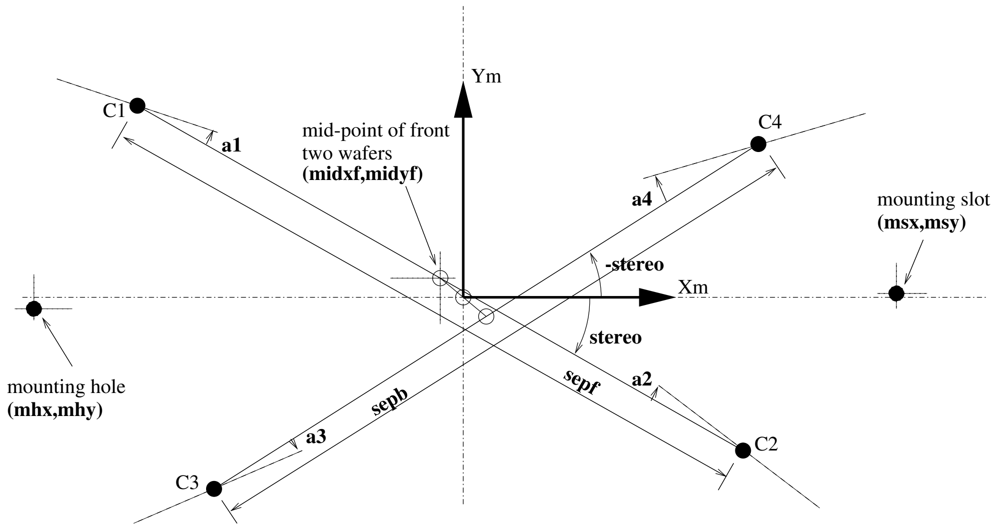

Figure 1: Definition of the parameters which describe the geometry of a standard module. Black circles C1 to C4 are the centers of the four wafers where center is defined as the intersection of the two mid-lines. The dashed line through each center gives the measured orientation of each wafer. Open circles are the center points of lines. The module is described in the database with 13 numbers: three coordinate pairs in the X_m, Y_m system (**mhx,mhy**), (**msx,msy**) and (**midxf,midyf**), two wafer separations **sepf**, **sepb** the angle **stereo** and four wafer angles **a1, a2, a3, a4**. Stereo angle is measured from the X_m axis and wafer angles from the stereo axis, with anti-clockwise rotation being positive.

We then argue that the main difficulty with space point alignment will be to know where the module is. Only a small part of the error budget should be used up on uncertainty about the relative positions of the wafers within a module. So we arbitrarily divide the above values by three to get a target value for internal wafer alignment within modules.

The in-plane alignment of the four wafers and two mounting holes of a module are described by the 13 parameters defined in Figure 1. Nine of these parameters describe the relative positions of the four wafers and the tolerances of these nine are chosen so that thier combined effect is a 4 micron r.m.s. on the space point in the ϕ direction. Table 2 shows how each of these parameters contributes to the ϕ resolution, under the assumption that the parameters will have a top hat distribution between the tolerance limits.

The out-of-plane alignment of the module is similarly calculated by taking one third of the 200 microns r.m.s. value and then choosing the top hat distribution with the same r.m.s., which gives a tolerance of ± 115 microns.

For the in-plane alignment of the two mounting holes we choose a tolerance of ± 20 microns in the ϕ direction. This is governed by our need to guarantee adequate overlap between adjacent modules for alignment with tracks [5].

5 Detector heat load

There are two sources of heat load on the detectors; electrical power supplied by the detector bias voltage $\times$ leakage current and heat transferred from the environment by convection and radiation. The first is a strongly rising function of detector temperature which can lead to thermal runaway, while the second is a weakly falling function of temperature.

5.1 Detector electrical power density

The following information is used to derive the maximum power that we think could be generated in the detectors after the full 10 years of running for which ATLAS is designed.

We assume a maximum detector bias of 460 V, derived from a maximum of 500 V supplied to the module with a drop of 40 V in the filter. After irradiation the detector leakage current is normally dominated by current generated thermally in the bulk of the silicon, but there can also be contributions from surface currents and from breakdown. We base our estimate of leakage current on a sample of pre-series forward SCT detectors which includes all the different detector geometries and two manufacturers. The detectors were irradiated with 24 GeV protons to a dose of 3.0×10^{14} cm^{-2}, annealed for 7 days at 25 C, then measured at 350 V and -18 C. Three detectors which showed clear signs of breakdown were excluded from the sample. Any surface current which may have been present was included in the measurement. The typical current, normalised to detector area was 0.034 A/m^2 and a safe upper limit which covers all the detectors in the sample with some safety margin was 0.043 A/m^2. To take account of the slight current rise that is observed between 350 and 460 V we add 5 % to get 0.045 A/m^2.

We use a hardness factor of 0.51 [9] for the relative damage caused by a 24 GeV proton, compared with the standard 1 MeV neutron. For the temperature dependence of the leakage current we use the relation $I(T) \propto T^2 \exp(-E_g/2KT)$ with $E_g = 1.2$ eV. This energy gap is larger than the standard value for silicon but it matches our measurements better. Designing for a large E_g value is safe in that it leads to a faster evolution of power with temperature and more tendency for runaway.

We use the most recent calculation of radiation levels in the inner detector [8]. This predicts that the maximum is in disk 9 which will receive 1.8×10^{13} 1 MeV neutrons/cm^2 per full luminosity year. The level is almost equally high in the inner detectors of disks 1-6. The estimated uncertainty on this value is $\pm 50\%$ which is made up from about $\pm 30\%$ from the *pp* inelastic cross section and multiplicity, with the remainder due to the particle transport simulations and damage constants.

With all the above information we arrive at a specified power density of 185 W/m^2 at 0 C. In terms of the alpha parameter which is frequently used to describe radiation induced leakage current, this is equivalent to $\alpha = 4.7 \times 10^{-17}$ Amps per 1 MeV neutron cm at 20 C.

5.2 Heat load from the environment

The design chosen for the forward module is one which attempts to provide two separate heat paths to the coolant, one for the high powered hybrid and another for the lower powered detectors. This is done rather successfully within the module itself but it has the consequence that we must be careful to evaluate the "cross-talk" which occurs in the cooling block and via the environment. The cooling block is the subject of tests and simulations described elsewhere. Heat lost from the hybrid by convection and radiation tends to be picked up by the detectors because they have large area and low temperature. We have estimated this heat flux in three complementary ways and found reasonable agreement.

Firstly we have used textbook formulae for the transfer of heat by convection from simple shaped surfaces in an environment of uniform temperature [10]. These have been refined by summing over the range of different orientations of the heat sources (hybrids) and sinks (detectors) which are present on the disk [11]. Requiring heat balance in the gas fixes the average gas temperature at around -1 C and the load on the front face detectors by convection is then estimated to be about 0.35 W on an outer module. The detectors on the back of a module which face the disk are not expected to receive much heat by convection because the gas there is trapped in a layer less than 1 cm thick and is baffled by a lot of cooling pipes and cables, so it can not form efficient convection cells. The power cables themselves dissipate heat of about 0.25 W per module. The cables run underneath the outer ring modules and cooling pipes. Some of the cable heat will be absorbed directly by the cooling pipes but some will get into the detectors. We estimate that the total convection heat picked up by the back-face detectors will be no more than 0.2 W per module. Radiation is expected to be a smaller source of detector heating than convection but not completely negligible.

Secondly, we have investigated the convective heat load on the front-face detectors with a computational fluid dynamics (CFD) simulation [12]. A very simplified geometry was used to represent the space between two disks where gas can flow freely. The walls of this space were given a fixed temperature at the places where they are tiled with modules and assumed to be insulating elsewhere. The module temperatures were assumed to be a function of radius only, i.e. independednt of azimuth. The CFD simulation predicts a plausible-looking pattern of gas flow and heat transfer. The heat transfer to outer modules varies from 0.04 W at the bottom of the ring to 0.55 W at the top of the

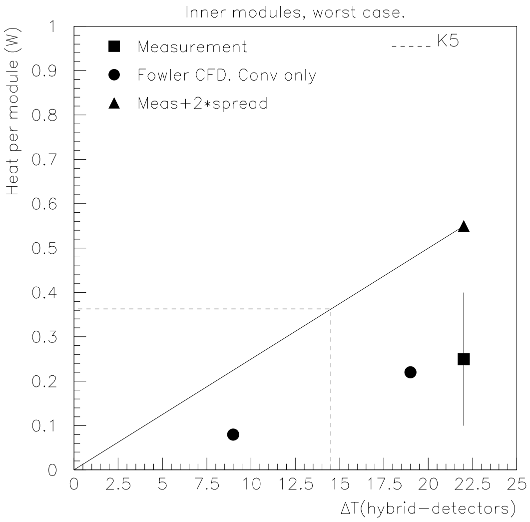

Figure 2: Summary of convection results for inner modules, showing extrapolation of the upper limit heat load to the expected detector-hybrid temperature difference of 14.5 degrees.

ring. Middle modules show a similar pattern to outers, with the range being from 0.16 to 0.55 W. Inner modules show the opposite pattern with the largest load being 0.22 W on the lowest modules and falling to 0.03 W at the top. This CFD simulation shows that the order of magnitude of the textbook estimates was right but that there is significant variation with position. It says nothing about the backward facing detectors or the effect of radiation.

Finally, we have built a thermal mock-up [13] of a pair of facing disks and measured the heat picked up by the components representing the detectors. The mock-up includes the real pattern of high and low modules. The dummy detectors are connected to cooling pipes and the dummy hybrids are electrically heated to about 22 degrees above the detectors temperature. An effort has been made to use materials with appropriate emissivities. The disks are represented with insulating foam covered with aluminium foil of the appropriate thickness to mimic the conductivity of the carbon fibre skin. We find that the heat picked up by outer modules is largest when the module is at the top of the wheel and is significantly larger for modules on high blocks than for those on low blocks. For these modules in the worst position, the average heating was 0.6 W with a measurement spread of 0.1 W. The pattern and magnitude of heat picked up by middle modules was very similar to that seen in outer modules, so we take it to be exactly the same. The power picked up by inner modules shows a rather large spread. There is some hint of the pattern seen in the CFD model where inner modules at the bottom of the wheel see the most heat. The average power of inners on high blocks is 0.25 W with a spread of 0.15 W. An attempt to measure the heating caused by dummy power tapes gave no significant result. All that we can say is that their effect is to add less than 0.1 W to the heat going into outer modules. We do not expect any effect on middle or inner modules because the power tapes do not pass underneath them.

Figures 2 and 3 summarise results from the mock-up and the CFD calculation. We take the measured power plus twice the spread of the experimental results plus 0.1 W to account for the heating by power tapes to be a safe upper limit. It is necessary to be quite conservative here because the mock-up measurement differs from the real SCT in many details. We do a linear extrapolation downwards from the measured hybrid-detector temperature difference to the one expected in reality. Some further results from the mock-up which are not reported in [13] support the validity of the linear extrapolation. In fact one expects convective heat transfer to be slightly more than linear in ΔT and the CFD result shows this effect, so linear extrapolation downwards is safe. We conclude that the specification for convection plus radiation heat load should be 0.8 W for outer and middle modules

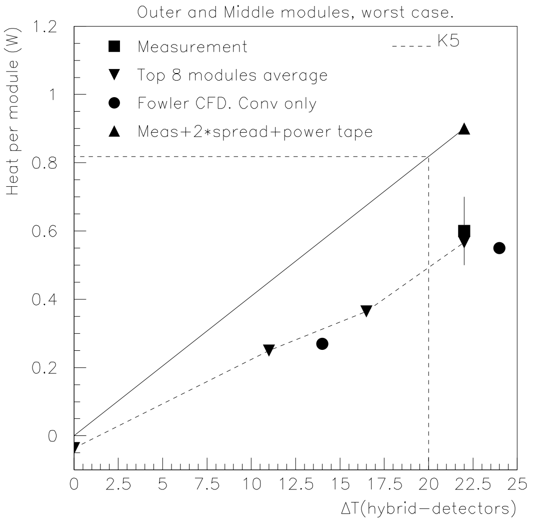

Figure 3: Summary of convection results for middle and outer modules, showing extrapolation of the upper limit heat load to the expected detector-hybrid temperature difference of 20 degrees. The measured value of 0.6 W is taken from [13] and the other set of points at a range of hybrid temperatures was measured later with the same mock-up, averaging results from eight outer modules at the top of the disc.

and 0.4 W for inner modules.

6 Hybrid power

From Alex Grillo

There are two different power specifications for the ASICs because there is a substantial difference between the power consumed by the chips in normal operation and the amount that could be consumed in diagnostic or turn-on modes. We are specifying the power supplies to provide the larger amounts in order to make sure that the diagnostic modes can be exercised if desired and that the power supplies will not trip if the ASICs should power up in a state which draws more current than normal operation.

The lower power specification, appropriate for cooling calculations, covers worst case process variations of the chips and maximum operating voltage (4.2V). The plan would be to set the programmable current limit on the power supplies at this lower level but maintain the hardware trip point at the higher level discussed in the paragraph above. The programmable limit would be raised to the higher limit only if the diagnostic mode is needed and then immediately set back to the lower limit. For the overall cooling capacity it would be safe to assume no more than one module operating at the higher level and all others operating at the lower limit. The power values are shown in Table 3.

	Power Suppy Spec.	Cooling System Spec.
Master ABCD	0.754 W	0.580 W
Slave ABCD	0.661 W	0.488 W
Opto Links	0.72 W	0.72 W
Total	8.84 W	6.76 W

Table 3: Maximum hybrid power specifications.

7 Expected Thermal Performance

After years of experience at measuring, simulating and iterating the module design we are now able to predict the thermal performance of a given design with reasonable accuracy. In general it requires a detailed finite element analysis (FEA) simulation to answer any question fully. But we have found that there is a simple model which describes detector temperature and thermal runaway to within a few percent. We describe the model here and use it later on.

The problem with an exact solution is that power input to the detector at a given point is a function of temperature at that point. And temperature at one point is a function of power inputs at all points. However the forward module design is one that connects all points on the detectors with low thermal resistances via the silicon and TPG, so there is not much variation of temperature across the detectors. The dominant thermal resistance is common to all parts of the detectors and is between the detectors and the cooling fluid.

So an approximate solution is to assume that all points on the detectors are at a common temperature which is the average of the real temperature distribution. The relation between this average temperature and the total power is calculated with one of the FEA programs, using a uniform power input over the detector area. The relation is strictly linear and is referred to as the thermal resistance of the system. It is often convenient to split this up into two parts; the "module thermal resistance" between the detectors and the cooling block surface and the "block thermal resistance" between the block surface and the coolant. For the purpose of the FDR we are specifying the block surface temperatures at maximum power load so we do not need to go into detail about the blocks. However it is worth noting that the main cooling block connects both hybrid and detector power to the coolant and can be described by a network of three thermal resistances. The far-end block can be represented by a single thermal resistance.

The accuracy of the model is demonstrated as follows. With uniform power load of 1 W on an inner module the FEA program predicts that the detector temperatures range from 3.76 to 5.11 with an average of 4.53 degrees above the temperature of the block surface. When we run the same simulation with the real temperature dependent power distribution, adjusted so that the total power is again 1 W, we find that the detector temperatures range from 3.74 to 5.15 with an average of 4.54. These results, and equivalent numbers for the outer module at 2 W are shown in Table 4. This justifies our use of the module thermal resitance as the single parameter which defines the thermal performance of a module to a very good approximation.

	Minimum temperature	Maximum temperature	Average temperature
Inner module, Uniform 1 W load	3.76	5.11	4.53
Inner module, T dependent 1 W load	3.74	5.15	4.54
Outer module, uniform 2 W load	3.38	5.07	4.43
Outer module, T dependent 2 W load	3.35	5.13	4.45

Table 4: Temperature ranges and average values simulated with different power distributions. This shows that it makes little difference to the module thermal resistance whether the detector power is uniformly distributed or has the real teperature dependent distribution.

8 Thermal Performance Simulations

The thermal performance of forward SCT modules has been simulated with three different FEA programs. In principle one is solving the equilibrium heat flow equation in a three dimensional object with well defined boundary conditions, which ought to be straightforward. However, there are two features which add to the difficulty in this case. Firstly, the exponential increase of detector power with temperature makes the problem increasingly non-linear as one gets close to thermal runaway. Secondly, the module includes some thin layers of glue which are an important barrier to heat flow, so they must be resolved by the mesh, which pushes up the number of cells and/or the aspect ratio of the cells.

The use of more than one FEA package for these simulations has allowed us to understand the thermal performance rather well. The main features of each pacakage and the way the module has been modelled in each case is described below.

8.1 ANSYS

The ANSYS model is fully 3 dimensional with seperate elements for each different layer of material in the module except for the copper/kapton circuit which is modelled with just one average material. The outer module model has 13607 elements and 17963 nodes. The grease layer, which is really 0.03mm, is scaled up to 0.1mm with its conductivity scaled down proportionally so as to avoid very thin layers. The next thinnest element is the AlN-TPG glue layer at 0.05mm which is modelled at its true thickness. The largest aspect ratio of any element is 54:1.

The model is run in the transient mode for 2000 simulated seconds and the step size is 40 seconds. At the end of the run there may be a small difference between the input and output power. This diference grows to a few percent as the module gets close to runaway. When the module is clearly in runaway the program crashes before reaching 2000 seconds.

8.2 A model written specifically for this problem (MPI)

The thermal properties are simulated using FEA analysis. The module is described by a grid. Each cell i is characterized by:

- The thermal conductivities C_{ij} between the cell and its neighbors $j = 1, 6$. This conductivity depends on the thermal conductivity of the cell material and the material between the cell, the cross section of the cell boundary, and the spacing between two adjacent cells.
- A heat source P_i in case the cell is made from detector silicon or is a readout chip.
- The cell temperature T_i

The detector part of a module is divided into 55 times 28 cells (in the module plane) and 4 cells (layers) in z. The hybrid part has 28 times 33 cells and 4 layers in z. Cell spacing is not equidistant but varies to reflect local complications of the module, e.g. the cooling point uses more cells per area than the silicon region between the support structures.
The four layers in z reflect the module layers:

1. Silicon
2. TPG (central spine) or AlN (wings)
3. TPG (central spine) or AlN (wings, cooling block contacts)
4. Silicon

The glue layers between the different materials are described by including their thermal resistivity in the C_{ij} between the layers. The module is cooled entirely by the cooling blocks. No heat transfer to and from the ambient gas is foreseen ($C_{ij} = 0$ at those boundaries). The cooling block properties are described in Section 9.3.
The temperature dependence of the silicon power density in cell i is modeled using:

$$P(T)_i = P_0 \frac{T_i^2 \exp\left(-\frac{E_g}{2kT_i}\right)}{T_0^2 \exp\left(-\frac{E_g}{2kT_0}\right)} \tag{1}$$

For silicon, the nominal band gap is $E_g = 1.1$ eV. Measurements of irradiated silicon detectors indicate a slightly larger value ranging from 1.15 to 1.26 eV. As worst case 1.26 eV is used in the calculations. The ASIC chips have a constant power density.
Now for each cell the temperature T_i is calculated by demanding local heat balance:

$$\Sigma_{j=1}^{6} C_{ij}(T_j - T_i) + P_i = 0 \tag{2}$$

These calculations are iterated until the largest temperature change is below a certain value and the heat generated in the modules equals the heat collected at the cooling points.

8.3 FlexPDE

The FlexPDE package [14] uses the FEA method to solve partial differential equations (PDEs) in two or three dimensions. It knows nothing about the laws of physics, the user has to put in the appropriate equations and boundary conditions. It can cope with a large number of linked PDEs relating different variables. It has adaptive re-gridding and it can deal with non-linear problems. Its chief limitation is that the quantity which it solves for must be continuous; not a problem in this case where we are solving for temperature.

We have found that it is a good approximation to treat the module as a two dimensional laminated structure. This depends on the fact that it is made up from thin layers with good thermal conductivity (which carry all of the heat flux in the x, y plane and have negligible temperature gradients in the z direction) alternating with even thinner layers of material with poor conductivity (which only transport heat in the z direction). Each layer, i, of the laminate has its own temperature field, T_i, which obeys the equation;

$$K_x \partial^2 T_i / \partial x^2 + K_y \partial^2 T_i / \partial y^2 + S_i = 0 \tag{3}$$

Where K is the product of the thermal conductivity and thickness of the layer. The source, S_i, contains a term for power generation within the layer, which may be constant for the readout chips or temperature dependent for the detector wafers. A layer which is in contact with a cooling block also has a term, $(T_{block} - T_i)H_{grease}$, which describes heat flow from the layer into the cooling block via the grease. Finally, S_i contains terms like $(T_j - T_i)H_{ij}$ which describe heat flow between layers through a contact medium such as glue, where H_{ij} is the glue conductivity divided by its thickness. Of course there must be a matching term $(T_i - T_j)H_{ij}$ in the equation for the neighbouring layer, j.

The most difficult part of the module to simulate accurately with this laminate approximation is the end of the spine where 0.225 mm of TPG is glued onto 0.225 mm of AlN and the AlN is in contact with the cooling block via a 0.03 mm grease layer. By comparison with a three dimensional model of this area we have shown [15] that the laminate approximation could introduce an error of order 0.2 K/W into the thermal resistance between the detectors and the coolant. This translates to an uncertainty of ± 15 $\mathrm{Wm^{-2}K^{-1}}$ in the power at which runaway occurs.

9 Inputs to the FEA models

The geometry of the modules was taken from the drawings [1], with the exception that the simulations include the shunt shield which was integrated with the hybrid but has now been dropped from the final design. In all simulations the interface between the module and cooling block is a 30 micron layer of thermal grease. Some simplifications of the geometry are necessary but they are not expected to have any impact on the thermal performance. The level of detail which has been modelled can be seen in Figures 4 and 5.

9.1 Power Input

Simulations are run with a total heat load on the hybrid of 7 W. This load is distributed uniformly over the 12 readout chips. We ignore the fact that a small part of it is really generated in other components on the hybrid.

Several runs of the simulation are done with different values of the detector electrical power from zero up to the power which causes runaway. The simulations are run with an additional load of 0.4 W for inner modules (or 0.8 W for outer modules) which is distributed uniformly over the detector surface and represents an upper limit on the heat which can be picked up from the environment by convection and radiation.

9.2 Materials

All three simulations use the material properties which are shown in Table 5. All conductivities are taken from manufacturer's data apart from the glues [16] and the TPG [17] which are based on our own measurements. The glue between detectors and spine requires some explanation. Modules are built to a fixed thickness, so variations in detector and spine thickness are taken up by this glue and its resulting thickness is 90 ± 40 microns. In order to avoid glue being sqeezed out when the gap is at its minimum thickness we have to accept a low coverage when the gap is at its maximum thickness. The coverage turns out to be 35% at 130 microns thickness and it is this worst case which we use in the simulation.

Thickness (mm)	Conductivity in x/y/z ($Wm^{-1}K^{-1}$)	Description
0.5	180	AlN cross bars
0.225	180	Thinned AlN where it overlaps TPG, also in thermal plugs
0.5	1700/1700/8	TPG spine
0.225	1700/1700/8	Thinned TPG where it overlaps with AlN
0.01	0.2	Parylene coating on TPG
0.285	136	Silicon Detectors
0.3	136	Front end chips
1.0	0.25	Stesalit location washers
0.3	1.5	Fan-in glass substrate
0.001	200	Aluminium tracks on fan-in
0.03	0.42	Thermal grease between block and module
0.05	1.8	Elastosil glue between AlN and TPG
0.125	10.	Glue between chips and thermal plug
0.13	0.2	Araldite 2011 glue. Assume 35 % coverage in the space between the detectors and the spine
0.376	0.14	Kapton part of flex, including glue foil
0.048	400.	Copper part of flex, averaged
0.5	30/700/30	Carbon-carbon hybrid substrate
0.075	2.0	Glue foil in shunt shield and under thermal plugs

Table 5: Thermal properties of materials used in module construction.

9.3 Cooling Blocks

Our basic specification for the cooling blocks defines their surface temperature at two different power loads, as shown in Table 6. We will show that the module meets its specifications provided that the block meets these specifications. When running a module simulation it is useful to also have a model of the cooling block in which the surface temperature is a realistic, continuous function of the power load. Therefore the MPI and FlexPDE simulations make use of a simple model for the cooling blocks which is based on measurements of an earlier version of the cooling system and on the expected performance of the final version. The main cooling block surface is split into one part which cools the hybrid ($_h$) and another part which cools the detectors ($_d$). The relation between the temperature (T) and the power (P) flowing through these two surfaces is

$$T_h = 1.15P_h + 0.9P_d \qquad \text{and} \qquad T_d = 1.3P_d + 0.9P_h \tag{4}$$

where temperatures are measured relative to the coolant. For the far end cooling block a thermal resistance of 3.0 K/W is used. Table 6 shows that with a coolant temperature of -21 C this model matches the block specifications.

The Ansys simulation was run with fixed block temperatures.

10 Simulation Results at Standard Loads

Tables 7 and 8 show the simulation results at the two specified load points for inner and outer modules. It is not necessary to simulate middle ring modules because they are almost identical to outer modules from a thermal point of view. We expect middle modules to have a slightly lower heat load by convection than outer modules because they are not inside the warmest volume of

Power (W)	T_h (C)		T_d (C)		T_{end} (C)	
$P_h/P_d/P_{end}$	Spec	Model	Spec	Model	Spec	Model
7 / 1 / 2	< -10	-12.05	< -13	-13.4	< -14	-15
7 / 2 / 2	< -10	-11.15	< -12	-12.1	< -14	-15

Table 6: Cooling block surface temperature at the two specified loads.

nitrogen which accumulates at the top of the disk and they do not have power tapes running under the detectors. We therefore expect middle modules to run slightly cooler than outer modules, given the same level of radiation damage.

	Maximum load			Overload		
Load conditions						
Hybrid power (W)	7			7		
Detector uniform power (W)	0.4			0.4		
Radiation damage (Wm^{-2} at 0 C)	185			240		
Block T_h/T_d (C)	-10 / -13			-10 / -12		
Results	FlexPDE	MPI	Ansys	FlexPDE	MPI	Ansys
Temperatures (C)						
Chip 1	5.3	5.7	5.8	5.3	5.8	5.8
Chip 2	8.7	8.1	9.2	8.7	8.3	9.3
Chip 3	10.3	9.7	10.8	10.3	9.3	10.8
Hybrid thermistor	2.6		6	2.7		6
Detector average	-8.3	-8.0	-8.5	-5.8	-5.8	-6.2
Detector maximum	-7.8	-7.3	-7.8	-5.1	-5.2	-5.4
Detector minimum	-9.0	-8.3	-9.1	-6.7	-6.6	-7.1
Powers (W)						
Into detectors	0.49+0.4	0.48+0.4	0.51+0.4	0.83+0.4	0.78+0.4	0.87+0.4
Out of hybrid block	6.82	6.66	6.81	6.85	6.68	6.83
Out of detector block	1.07	1.22	1.09	1.38	1.38	1.43

Table 7: Simulation results for an inner module at the two standard load conditions. The module specification requires the detector temperature to be below -7 C at the maximum load and it requires that there is no thermal runaway at the overload condition.

10.1 Safety Margin at Standard Loads

The previous section shows that both module types are within specification at the standard loads. This is suplemented by two further figures which show how the two specified parameters (runaway point and detector temperature) evolve as conditions are changed. Figure 8 shows the effect of changing coolant temperature. Figure 9 shows the effect of an additional thermal resistance in the heat path between the detectors and the coolant. These results are calculated with the simplified model described in Section 7.

10.2 Runaway Curves

In order to make realistic runaway curves which pass approximately through the two standard load points the FlexPDE and MPI simulations we use the block model described in Section 9.3 with coolant temperature of -21 C.

The Ansys simulation uses fixed block temperatures, set at the overload values of $T_h = -10$, $T_d = -12$ and $T_{end} = -14$ C, which means that it will pass exactly through the overload point. This is conservative because the power loads that it predicts on the blocks are always below the overload values whereas the block temperatures stay fixed at the overload values.

	Maximum load			Overload		
Load conditions						
Hybrid power (W)	7			7		
Detector uniform power (W)	0.8			0.8		
Radiation damage (Wm^{-2} at 0 C)	185			240		
Block $T_h/T_d/T_{end}$ (C)	-10 / -13 / -14			-10 / -12 / -14		
Results	FlexPDE	MPI	Ansys	FlexPDE	MPI	Ansys
Temperatures (C)						
Chip 1	5.2	6.9	5.8	5.3	6.9	5.8
Chip 2	8.7	9.4	9.2	8.7	9.5	9.2
Chip 3	10.2	10.3	10.8	10.3	10.4	10.8
Hybrid thermistor	2.6		6	2.7		6
Detector average	-8.8	-9.7	-8.5	-6.8	-8.2	-6.9
Detector maximum	-8.1	-8.9	-7.8	-5.7	-7.3	-5.9
Detector minimum	-10.3	-11.5	-9.1	-8.9	-10.7	-9.5
Powers (W)						
Into detectors	1.16+0.8	1.00+0.8	1.10+0.8	1.88+0.8	1.54+0.8	2.02+0.8
Out of hybrid block	6.82	6.74	6.81	6.85	6.80	6.81
Out of detector block	0.95	0.96	1.13	1.17	1.14	1.22
Out of end block	1.20	1.10	0.96	1.67	1.40	1.79

Table 8: Simulation results of an outer module at the two standard load conditions. The module specification requires the detector temperature to be below -7 C at the maximum load and it requires that there is no thermal runaway at the overload condition.

All simulations are run with a range of electrical loads and as usual the hybrid load is 7 W, the convective load is 0.2 W per detector. The results are shown in Figures 6 and 7. For the inner module all three simulations show similar temperatures and powers and a runaway point between 320 and 400 Wm^2 at 0 C.

For the outer module all three simulations predict a runaway point between 300 and 350 Wm^2 at 0 C, but their temperatures and powers do not match so well. The main difference is between Ansys and the others, due to the different assumptions about the block. At low damage the power out of the far end block is about 0.8 W, so the FlexPDE and MPI simulations will take its temperature to be $-21 + 0.8 \times 3 = -18.6$ C, whereas the Ansys simulation has this block fixed at -14 C. This accounts for the big difference in average detector temperatures, which diminishes as the power out of the end block goes up.

There is also a small difference in the module thermal resistance predicted by MPI and FlexPDE. This is visible as the difference in temperature gradient versus damage in the low damage region of Figure 7. It directly causes the difference of runaway points predicted by these two programs.

11 Conclusion on Simulations

Our models predict detector temperatures at maximum load to be around -8.4 C on inner modules and -9 C on outer modules. We also find that at the overload condition all models find a stable solution, which means that the module is not in thermal runaway. Runaway does not occur until the detector pwer reaches a level around 300 to 400 W m^{-2} at 0 C. Thus our simulations predict that the module design meets the thermal specifications. The margin by which this design exceeds the specifications can be characterised as allowing either an extra 1.5 degrees on the cooling block temperature or an extra 30% in the thermal resistance between the detectors and the cooling block surface.

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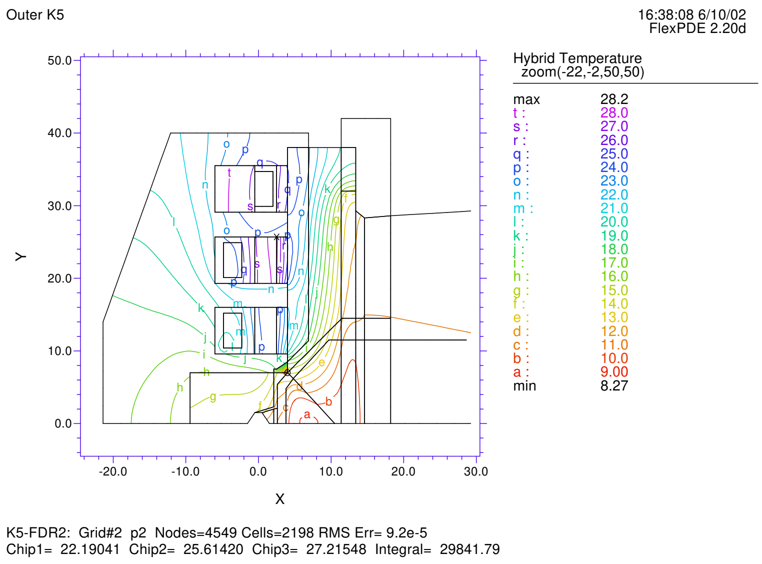

Figure 4: The temperature map of the hybrid region of an outer module simulated in FlexPDE. Temperatures are shown relative to the coolant. The load on the readout chips was 7 W.

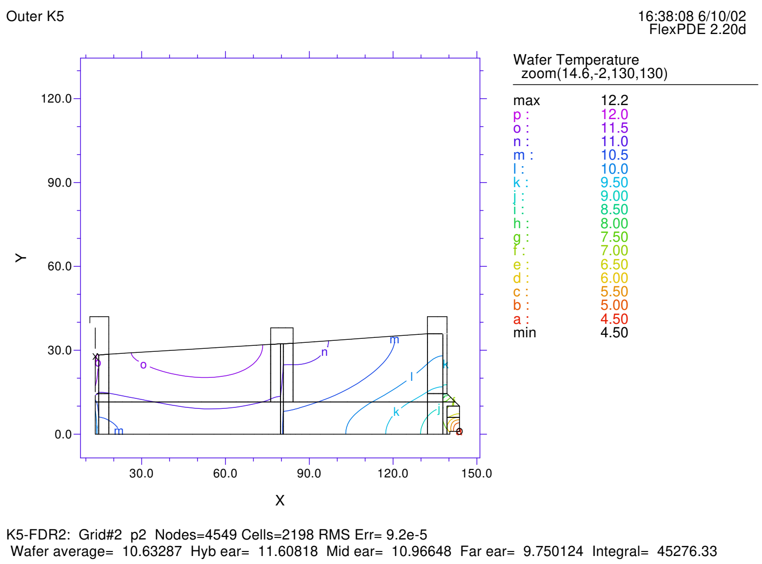

Figure 5: The temperature map of the detector region of an outer module simulated in FlexPDE. Temperatures are shown relative to the coolant which was at -21 C. The load on the detectors was 0.8 W uniformly distributed plus 240 Wm^{-2} at 0 C.

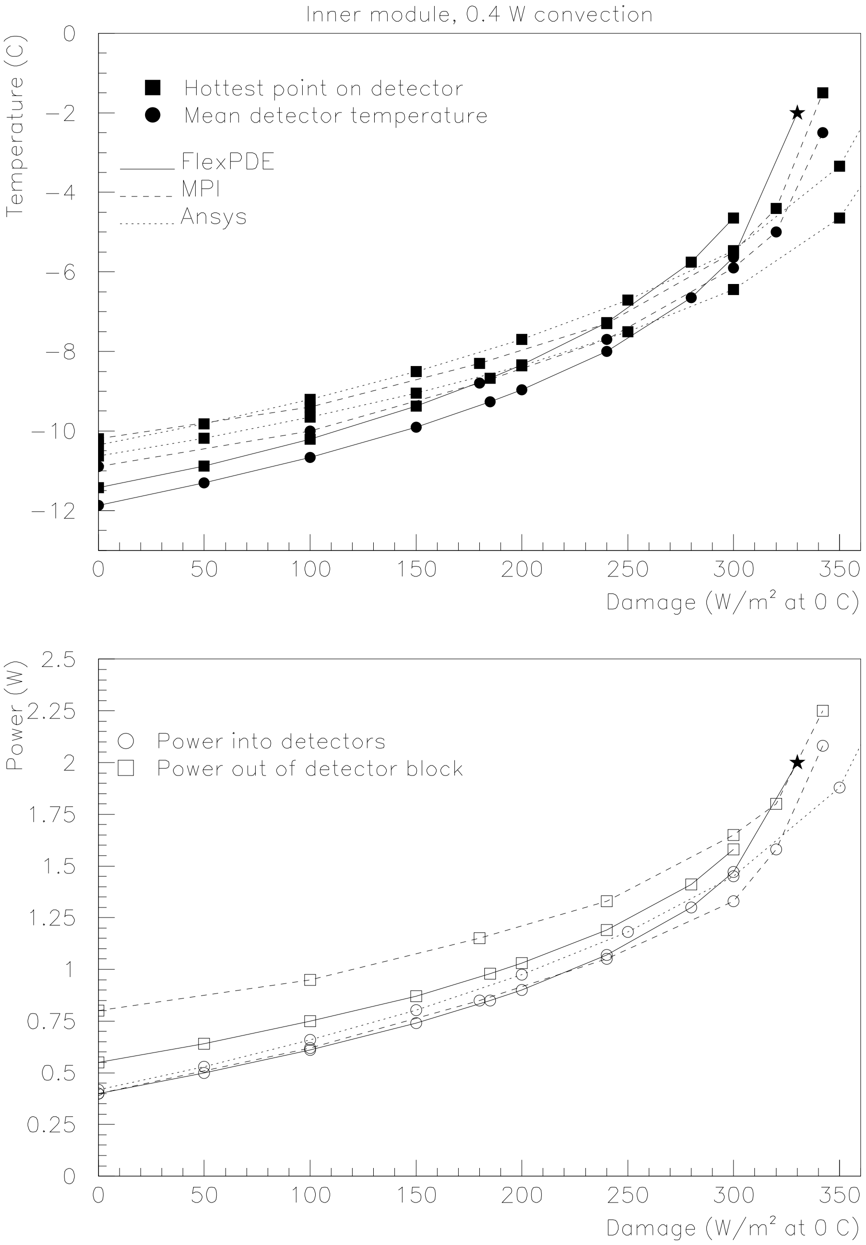

Figure 6: The inner module simulated with a coolant temperature of −21 C and a convective heat load of 0.4 W. The upper plot shows the detector temperature and the lower plot shows power generated in the detector and power flowing out through the detector part of the split cooling block. All points come from the full FEA simulations apart from the star which shows the runaway point and is based on an extrapolation of the other points.

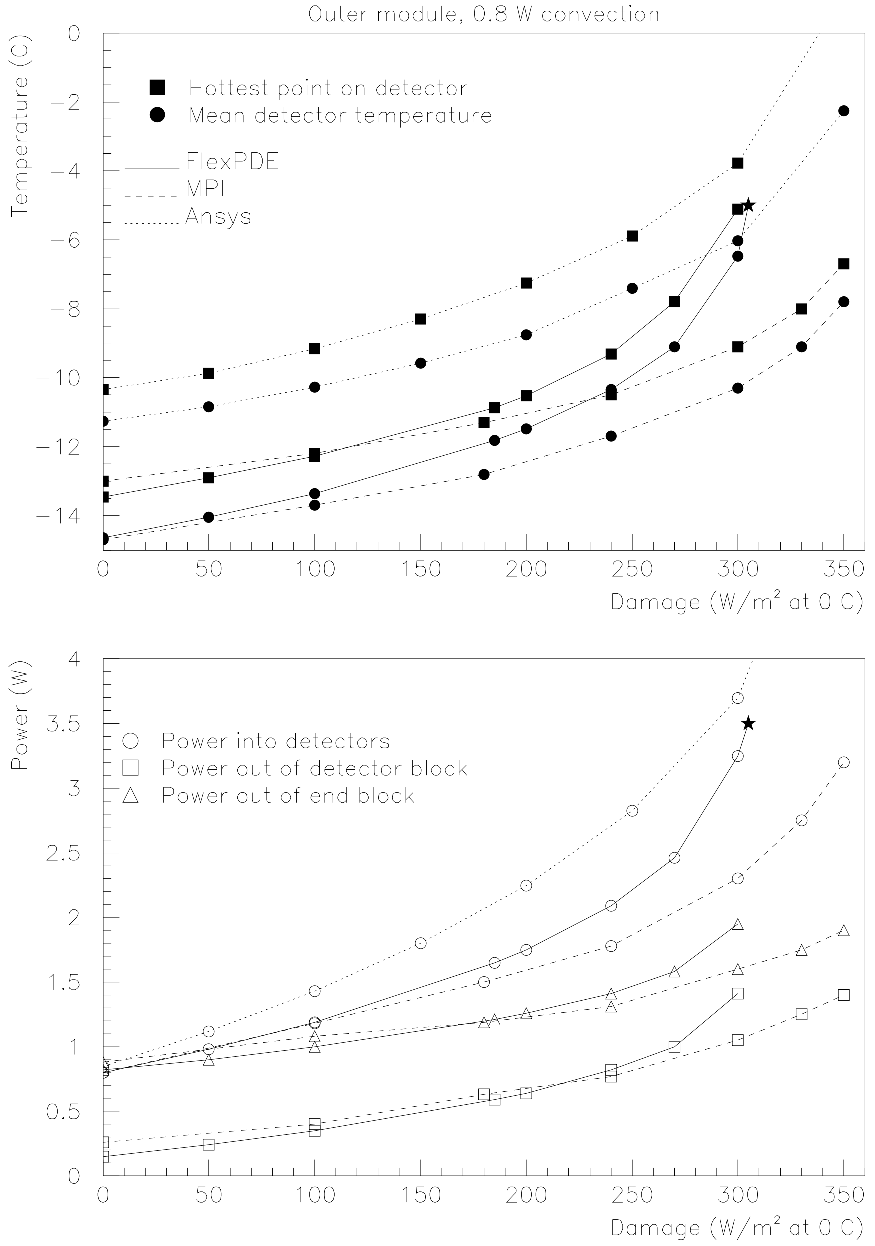

Figure 7: The outer module simulated with a coolant temperature of -21 C and a convective heat load of 0.8 W. The upper plot shows the detector temperature and the lower plot shows power generated in the detector and power flowing out through the detector part of the split cooling block and the end cooling block. All points come from the full FEA simulations apart from the star which shows the runaway point and is based on an extrapolation of the other points.

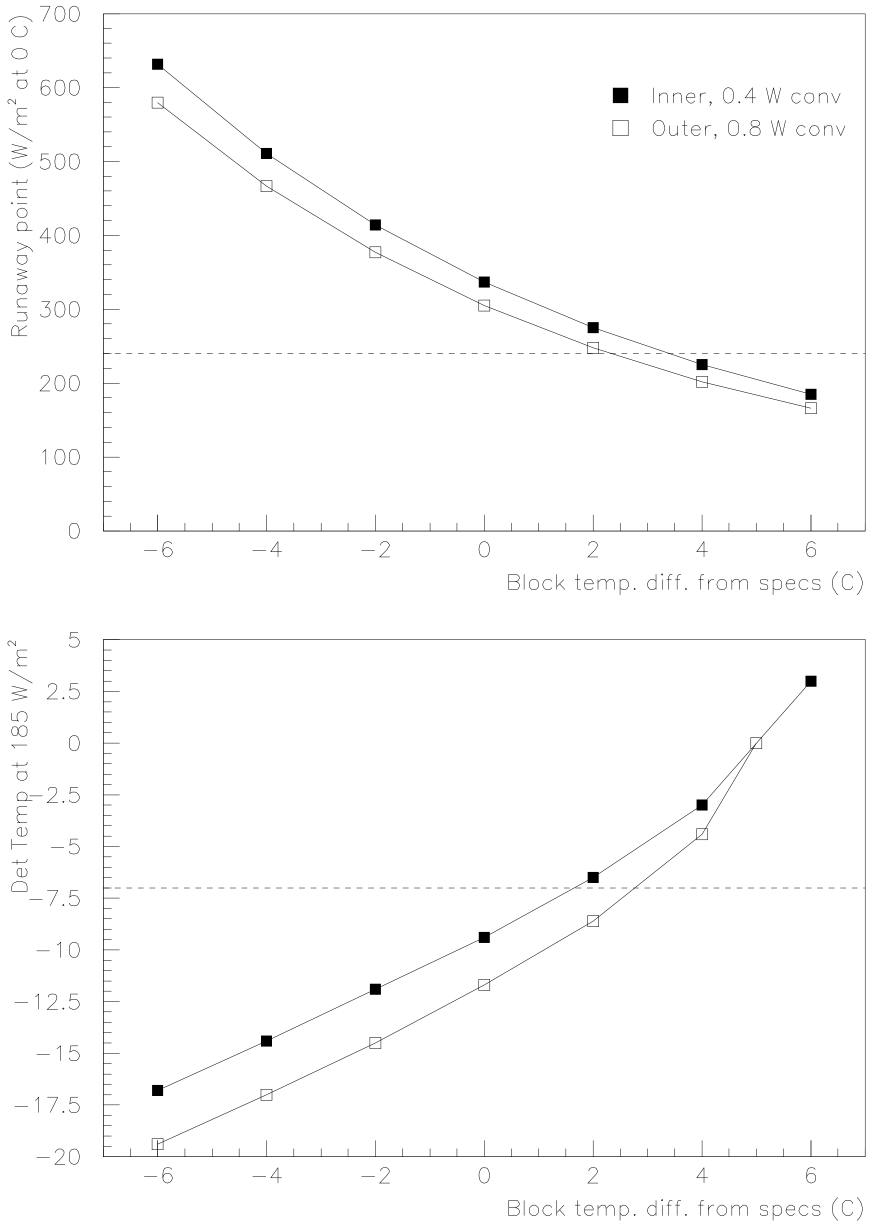

Figure 8: This shows how the module thermal performance changes as the cooling blocks are varied from their specified temperature. The upper plot shows the variation of the runaway point and the lower plot shows the variation of the detector temperature at the specified maximum load of 185 (Wm^{-2} at 0 C).

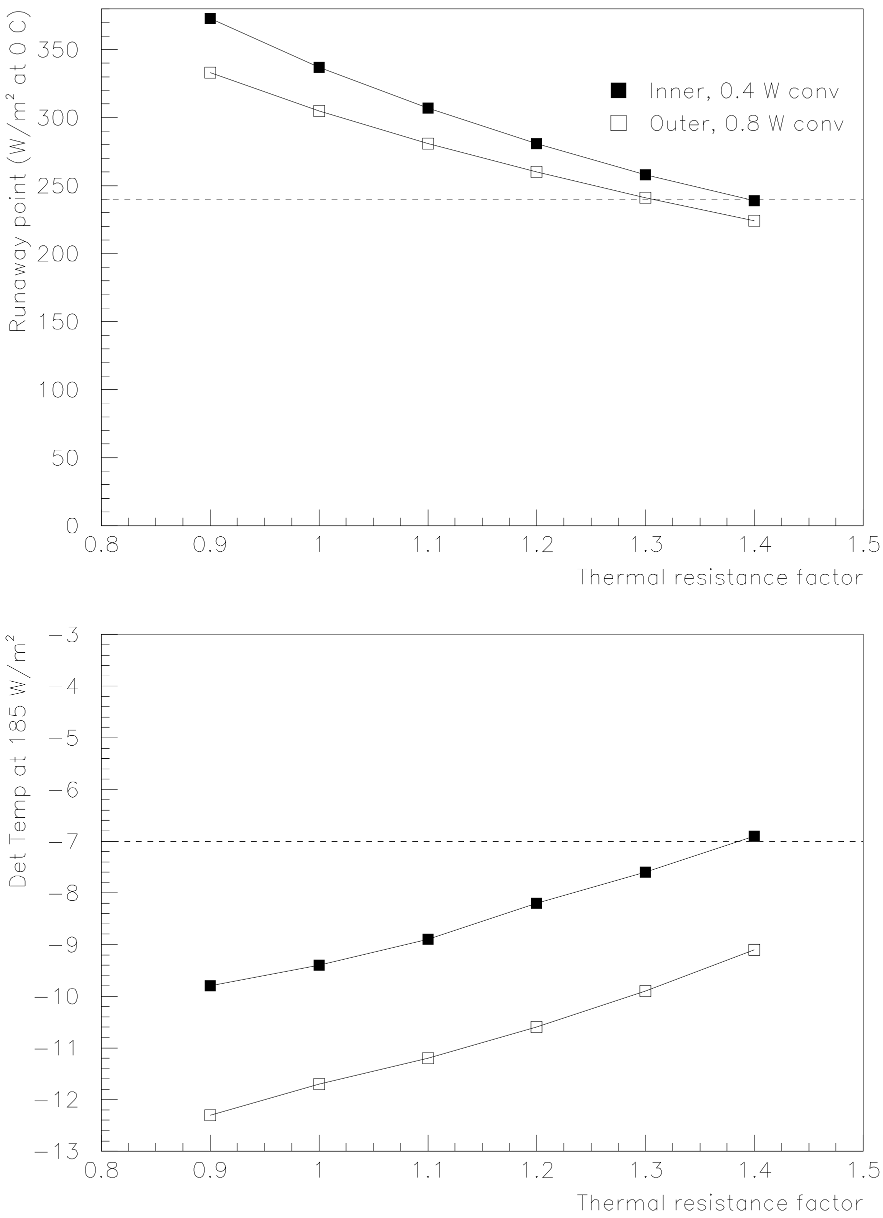

Figure 9: This shows how the module thermal performance is changed if the thermal resistance between the detectors and the cooling block is increased by up to 50%. The upper plot shows the variation of the runaway point and the lower plot shows the variation of the detector temperature at the specifed maximum load of 185 (Wm^{-2} at 0 C).