

Long-Term Irradiation Study of ABCD3TA ASICs

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Abstract

A long-term irradiation study was done on an ATLAS SCT barrel module hybrid with 12 front-end ASICs (ABCD3TA) to study the effect of a low dose rate irradiation on the ASIC's digital current (I_{dd}) consumption. This study was done at a ^{60}Co γ -source. The irradiation rate was measured to be 1.365 ± 0.045 rad/sec at a distance of 37.5 cm from the source. The hybrid received an accumulated dose of 10.91 Mrad over the course of 2200 hours of irradiation. Digital current, I_{dd} , increased from an initial value of 490 mA to a maximum of 900mA, proceeded to plateau around a value of 870mA and then dropped to below 800mA by the end of the experiment. The hybrid was allowed to anneal afterwards for several weeks and I_{dd} dropped to 600 mA. When compared to the higher dose rate tests performed at CERN, this demonstrates that the I_{dd} increase is much reduced at low dose rates and will be manageable by the SCT power supplies and cooling system if the problem does not get significantly worse with future fab lots.

1 Introduction

The ATLAS Semiconductor Tracker (SCT) community has adopted the ABCD chip, realized in rad-hard DMILL technology, as its choice for the front-end ASIC. Recent irradiation experiments done with the latest versionh of the chip, the ABCD3TA[1] at CERN PS (Proton Synchrotron)[2] and at X-ray sources[4] revealed significant increases in digital current consumption (I_{dd}). This was determined to be a DC leakage current, which increases with radiation damage. The cause was traced to structures in the IC, which emply two transistors with a common trench[3]. It is speculated that charges trapped in the oxide covering open a channel between the two transistors allowing the leakage current. Both

studies also showed evidence of short and long term annealing of the silicon oxide layer (an understood effect following irradiation of silicon).

Most chips involved in this study showed I_{dd} increasing from a factor of about two to over three for some chips. This raised concern that the current drawn by the SCT barrel modules would exceed the trip values of their power supplies or exceed the capacity of the cooling system. Both the CERN PS and X-ray experiments used a very high dose rate (X-ray, for example, used 36.6 krad/min) to expose the chips to the amount of radiation expected in the duration of the ATLAS experiment in a few hours. Correlation studies between the X-ray and CERN PS irradiations show a slightly smaller increase in I_{dd} at the PS irradiations which may be due to the slightly lower dose rate used there. It was hypothesized that using a lower dose rate (one closer to the rate anticipated at the actual ATLAS experiment) would allow for the annealing process to occur during irradiation, thus reducing the overall increase of I_{dd} [5]. A low-dose rate experiment to study these effects started at LBNL in late 2001.

2 Setup Overview

The irradiation tests were done on an ATLAS SCT K4 barrel hybrid (serial number 2022017000032) populated with 12 ABCD3TA chips. These chips were selected to represent the same wafers and lots that were used for chips that were irradiated at CERN PS and the X-ray irradiation (see Table 1).

Lot and Wafer	Chip number on hybrid (0 through 11)
Z34685, wafer 3, 5, 8	5, 0, 6
Z34685A, wafer 12, 20	7, 1
Z36459A, wafer 3, 4, 5, 6	2, 3, 4, 9
Z38850A, wafer 12, 15, 18	10, 8, 11

Table 1: Chips irradiated at LBNL ^{60}Co γ -source

This irradiation was done at the ^{60}Co source at LBNL. Because the radiation damage that causes the increase in current is due to ionization damage and not displacement damage, we can use a γ -source instead of a hadron source (such as the CERN PS). ^{60}Co has a half-life of 5.27 years and produces gamma rays with energy on the order of 1 MeV. The goal of the experiment was to expose the hybrid to 10 Mrad of radiation by the end of the run. The hybrid was placed at a distance of 37.5 cm from the source. The dose rate measured at this distance using calibrated Thermo-Luminescent Devices (TLDs) was 1.365 ± 0.045 rad/sec (see section 3.2).

The hybrid was placed on an aluminum holding fixture with coolant running through it, as seen in Figure 1. The coolant used was an approximately 50/50 mixture of water and anti-freeze (ethylene glycol). The coolant temperature was initially fixed at a temperature of 18°C and was later dropped to 16°C.

The hybrid and the cooling fixture were both placed inside an aluminum and lead box (cross section of $16 \times 16 \text{ cm}^2$) to stop low energy photons. The box was placed in front of the source in such a way that the center point of the hybrid is 37.5 cm from the centerline of the source (see Figure 1). Because the support card used for data readout is not radiation-hard, we used a custom-built extender cable to connect it to the hybrid, allowing enough space between the two to shield the support card.

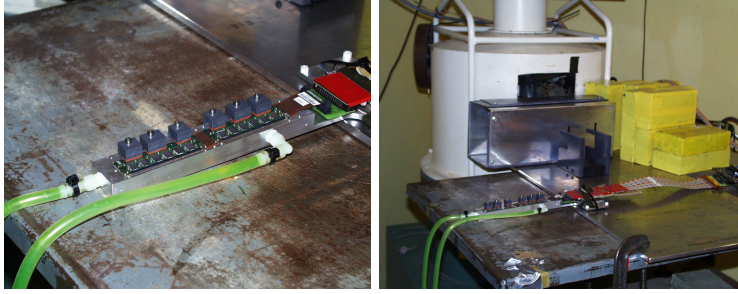


Figure 1: The hybrid with 12 ABCD chips on the aluminum cooling block (left) and with extender cable (right).

The support card is connected to a VME crate via a 10 m power cable (which connects to the SCT Low Voltage card) and a 10 m data cable. The VME crate is controlled by a PC running the SCTDAQ software[6]. The chips' performance before irradiation can be seen in Figure 2.

Digital Voltage (V_{dd})	3.98V
Digital Current (I_{dd})	490mA
Analog Voltage (V_{cc})	3.50V
Analog Current (I_{cc})	940mA

Table 2: Hybrid current consumption before irradiation

3 The Experiment

The irradiation experiment consisted of sequential 100-hour runs. During a run, the chips are continuously triggered and clocked. Both analog and digital voltage and current, and the hybrid temperature at the two thermistors T1 and T2 (see section 3.1) are recorded every five minutes. After each run, the chips' performance is tested for noise, gain, offset, and threshold levels.

Approximately three weeks into the test, the hybrid response showed unusual degradation. It was discovered that this failure was due to water condensation forming on the hybrid. After this incident, the hybrid was removed from the

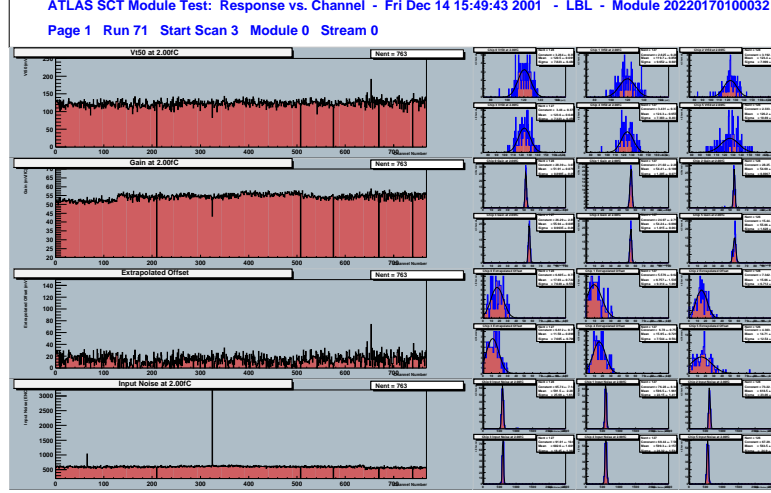


Figure 2: Channel summary before irradiation for first half of hybrid.

source and brought back to the lab for repair and drying. Several bonds from two of the chips were damaged and had to be repaired. The total service time used on account of this accident was 55 hours. During this period, the hybrid exhibited some annealing, with the digital current dropping from 760mA¹ to 720mA (the hybrid was kept at a temperature of about 20°C). After this incident, a continuous supply of dry air was provided to the hybrid.

3.1 Temperature Reading

It also became apparent that the hybrid temperature was reading several degrees lower than the temperature of the coolant. It was determined that this deviation was caused by a drop in voltage across the extender cable for the support card.

The SCTLV3 (low-voltage power supply) provides a digital voltage (V_{dd}) of 4.0V and an analog voltage (V_{cc}) of 3.5V. At point A (as shown in Figure 3), V_{dd} was measured to be 4.01V. At point B, it is measured to be 3.92V, representing a 90mV drop caused by the extender cable. Two thermistors, T1 and T2, are used to measure the temperature on the hybrid by the software (a thermistor is a resistor that varies its resistance depending on the ambient temperature). In normal operation, the SCTLV3 provides a current of 80 μ A to the two thermistors and in turn reads back the voltage drop across the two

¹All measurements of current have a digitization error of 5 mA

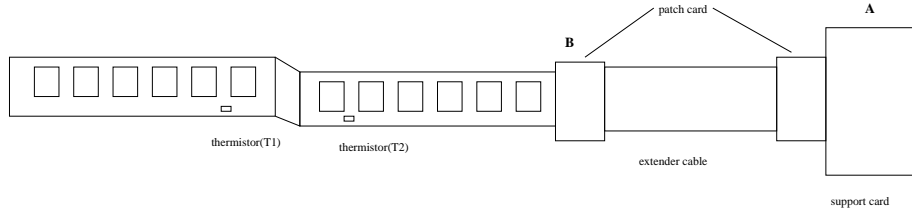


Figure 3: Voltage drop due to extender cable.

thermistors to determine the temperature they read. Due to the extraneous drop caused by the extender cable, the SCTLV3 and in turn the SCTDAQ software records a temperature that is several degrees lower than what is actually on the hybrid.

3.2 Dose Measurement

Initial measurement of the dose at the beginning of the run, using an electrometer², indicated a dose of 2 rad/sec. Subsequent measurements over the next few months, both by the LBNL ATLAS group and other experimenters using the ⁶⁰Co source indicated that the dose was actually lower.

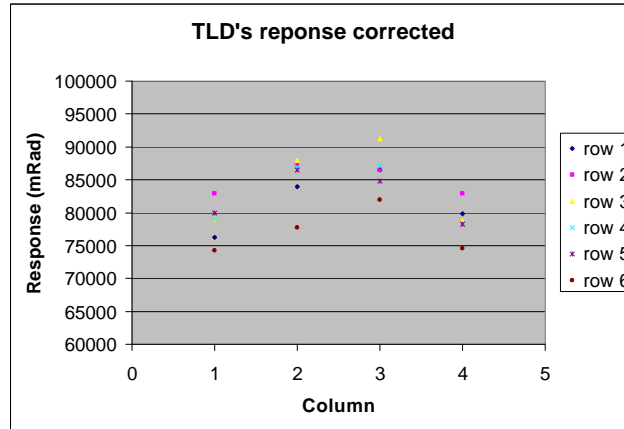


Figure 4: Corrected response of TLD array (66 s exposure)

To get a more accurate reading, a 4×6 array of Thermo-Luminescent Devices

²Victoreen R-meter, Model 570

(TLDs) were used. The TLD array was placed at a distance of 1.5 m from the center-line of the source and was exposed for 20.5 minutes per run. A total of four calibration runs were performed. The calibration runs yielded a dose of 101 Rad at a distance of 1.5 m for 20.5 minutes. The same array of TLDs was placed inside the box that normally houses the hybrid and was exposed to the source for 66 seconds. The results of that run can be seen in Figure 4.

Figure 4 shows that there is an edge-effect in the TLD array. However, since the dimensions of the hybrid correspond to the center four rows, we can be confident that the edge effect for our experiment is negligible. Therefore, the top and bottom rows of the TLD array were removed when calculating an average dose. Removing these two rows, averaging, and multiplying by the correction factor for silicon (1.0775) results in a dose rate for the chips on the hybrid of 1.365 ± 0.045 rad/sec. The error is due to the accuracy of TLD readings. This measured dose is closer to that estimated by other experimenters using the facility.

4 Results

The irradiation test commenced on December 13, 2001 and was concluded on March 16, 2002. At that time, the hybrid was brought back into the laboratory to commence annealing. The annealing lasted until May 13, 2002.

4.1 Irradiation

The total irradiation time was 2220.5 hours. Figure 5 shows a plot of overall dose (in Mrad) versus digital current. The data have the same qualitative pattern as seen in the X-ray study[4]. The current starts to rise after about 1 Mrad and it plateaus at 5 Mrad.

I_{dd} plateaued at 900 ± 10 mA at a radiation dose of 6.69 Mrad. This plateau lasted for 0.5 Mrad. The I_{dd} spontaneously dropped to 870 mA at a dose of 6.79 Mrad between runs (see Figure 5) following a brief hiatus in the run due to a software crash. The hardware was restarted with the assumption that power cycling the VME crate and the PC would solve the problem. Unfortunately, this was not the case. The I_{dd} remained within 10 mA of 870 mA for about 1.5 Mrad. At this point, the run was stopped to allow a biology experiment to use the ^{60}Co source. During this period, the chips exhibited some annealing: I_{dd} dropped to 830 mA and remained there for about 1 Mrad. The run crashed on 3/10/2002, due to the SCTLV3 (low-voltage power supply) inaccurately reporting an over-temperature alarm.

At the time of removal of the hybrid from the ^{60}Co facility, I_{dd} was at 790 mA. This is substantially lower than I_{dd} seen after 10 Mrad of irradiation at CERN PS or at the X-ray irradiations, which increased by a factor of two or three compared to the initial values.

Overall electrical performance (aside from digital current consumption) of the chips did not change much from before irradiation (Figure 2). Specific plots

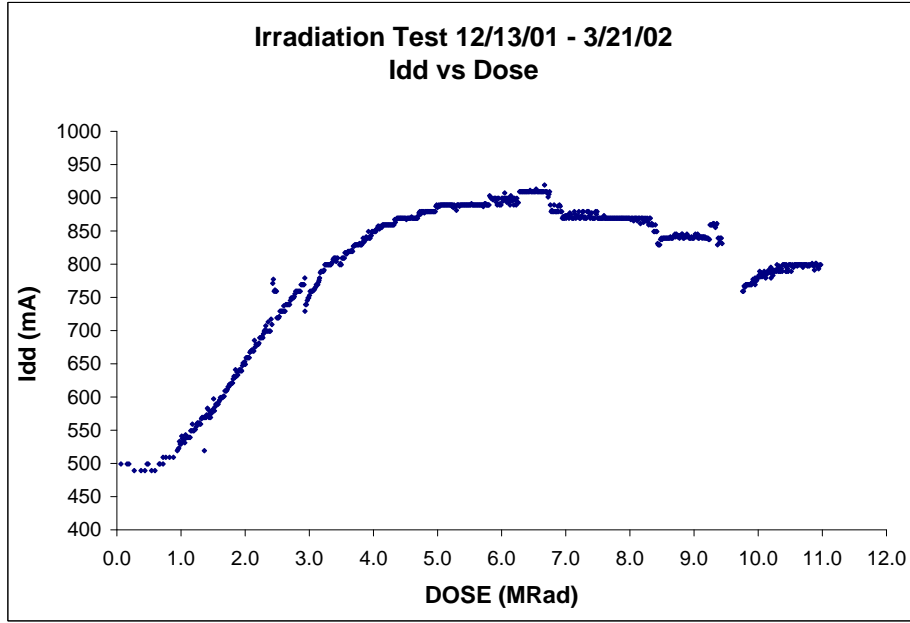


Figure 5: I_{dd} vs. Dose for entire irradiation experiment

of input noise, gain, threshold level and strobe delay register value settings (which are determined before each hybrid analog performance test) versus dose can be seen in Figure 6.

4.2 Annealing

The same test procedure was followed during the annealing as during the irradiation: the chips remained powered and triggered, readings of temperature and current were taken every five minutes and response curves were measured after every 100 hour run. The hybrid was kept at the same temperature, 18°C, as during the irradiation.

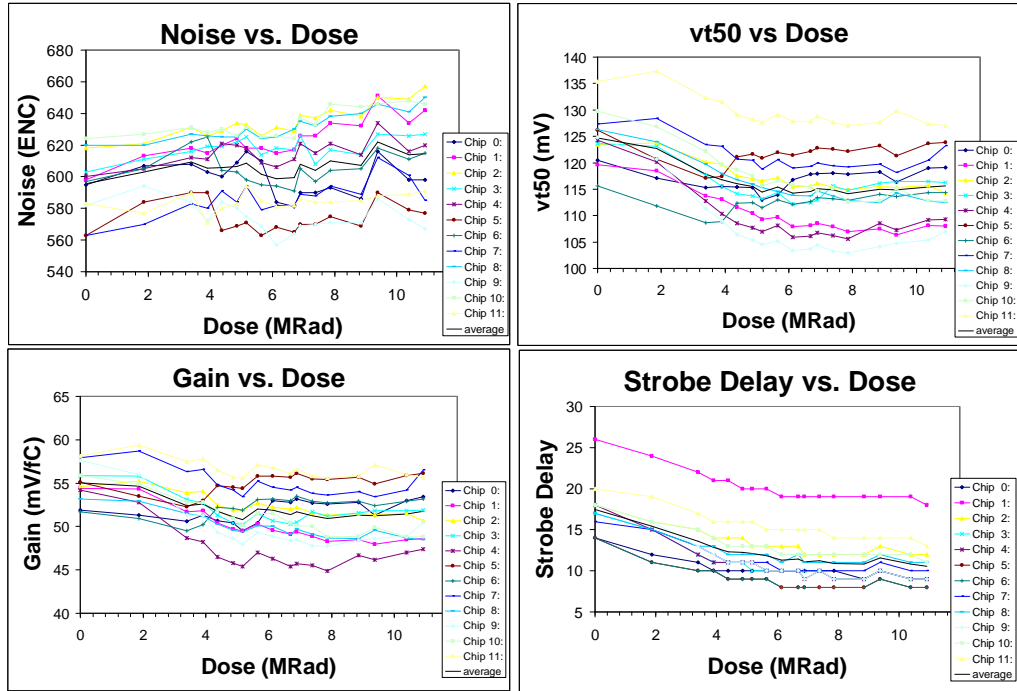


Figure 6: Input noise (top left), threshold level (top right), gain (bottom left), and strobe delay (bottom right) versus accumulated dose

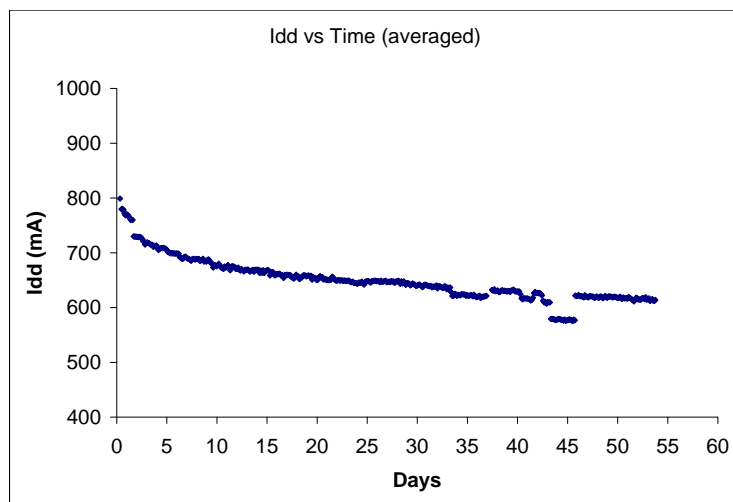


Figure 7: I_{dd} vs. Dose for entire annealing experiment

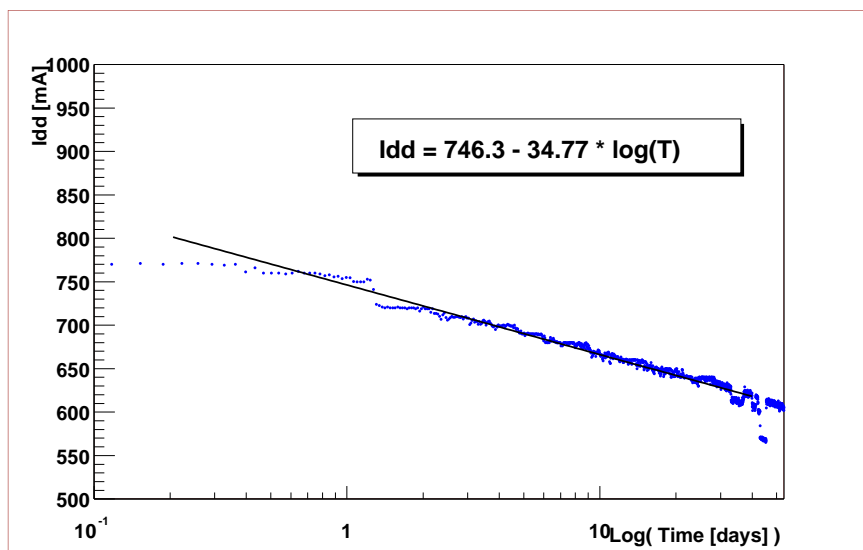


Figure 8: I_{dd} vs. Dose for entire annealing experiment (log plot)

Figure 7 shows a plot of digital current versus overall annealing time. At the end of 53 days of observation, I_{dd} dropped to 600 mA, only 16% above the pre-irradiation level. It has been long known that the annealing of the radiation-induced oxide- and interface-trapped charge in semiconductor devices is linear in log-time in limited time domain[7][8]. Figure 8 shows a plot of average digital current versus the logarithm of time annealed, fitted by a linear function. The fit results indicate normal annealing continuing for two months after the irradiation. We stopped the test because of the prohibitively large amount of time required to study the logarithmic dependence.

After the last set of measurements were taken for the entire hybrid, each chip was disconnected, one by one, to measure how much current each individual chip consumed. The results are summarized in Table 3.

Batch number	Wafer number	Chip number on hybrid	Final value of I_{dd} (mA)	% of total I_{dd}
Z34685	8	0 (master)	60	9.68
Z34685A	20	1 (slave)	50	8.06
Z36459A	3	2 (slave)	40	6.45
Z36459A	4	3 (slave)	60	9.68
Z36459A	5	4 (slave)	60	9.68
Z34685	3	5 (slave)	50	8.06
Z34685	5	6 (master)	50	8.06
Z34685A	12	7 (slave)	30	4.84
Z38850	15	8 (slave)	50	8.06
Z36459A	6	9 (slave)	60	9.68
Z38850	12	10 (slave)	40	6.45
Z38850	18	11 (slave)	50	8.06
Base			20	3.23
Total			620	100.00

Table 3: Chip by chip summary of post-annealing results. The base current consumption represents how much current is consumed by the hybrid with no chips connected.

5 Conclusion

We have performed the first low-dose irradiation experiment with ATLAS SCT front-end ASICs. The hybrid digital current consumption increased from an initial value of 490 mA to a maximum of 900 mA. Significant annealing effects were seen throughout and after the irradiation. It seems safe to conclude that the digital current consumption should not exceed a maximum of 1 A during the lifetime of the ATLAS experiment, since the dose rate that will be seen by SCT modules (0.05 rad/sec is expected) will be even less than that seen at our irradiation study. However, the contributions of wafer fabrication variations to this leakage current phenomenon are not understood. Indeed variations from lot to lot have been observed. It is, therefore, possible that the leakage current could be worse than measured here with other chips from other fab lots. This will need to be monitored during the fabrication period.

With proper monitoring against a significant worsening of this leakage current, the 1 A limit for Idd is within the power supply specification of 1.3 A and consistent with the cooling specifications of 10 W per module.

A Acknowledgements

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