Electrical Results from Prototype Modules

Abstract

This document describes the measured electrical readout performance of forward modules in the laboratory, in beam tests and in the SCT system test at CERN.

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1 Scope of the document.

The document summarizes results on the electrical performance of forward modules read out with the ABCD3T version of the SCT binary ASICs [1,2].

2 Performance goals of the modules.

The end-cap module electrical specifications are described in [3]. In brief, the modules need to fulfill the following conditions:

- Noise occupancy per strip < 5×10^{-4} after the full irradiation dose, 3×10^{14} protons/cm^2, which means that the minimum operational threshold needs to be set at 3.3 times the average RMS of the noise. An operating threshold of 1 fC would require an effective noise, considering electronics noise plus threshold spread, smaller than 1900 e^- ENC, yielding a median signal over noise ratio of 10:1, assuming a 3.3 fC signal at full depletion.
- Tracking efficiency > 99%.
- Capability to tag beam crossings.

These conditions translate into requirements on the module electrical and thermal stability, on the noise -to ensure the proper noise occupancy level-, on the front-end timing and on the proper matching of the channel discriminators in a single chip.

3 Available electrical modules.

In order to ascertain the electrical performance of the ATLAS SCT forward modules, a number of them have been built. Table 1 lists all the built modules, specifying which tests have been carried out on each of them.

Module	*Type*	*Hybrid type*	*Irradiated (3×10^{14} p/cm^2)*	*Data*			*Cal. factor*
				Lab. tests	*Test beam*	*System test.*	
K5-300	Middle	CICOREL		✓		✓	1.093
K5-301	Middle	CICOREL		✓	✓	✓	1.093
K5-302	Outer	CICOREL		✓	✓	✓	1.150
K5-303	Outer	CICOREL		✓		✓	1.171
K5-305	Outer	CICOREL	✓	✓	✓		1.171
K5-308	Outer	CICOREL	✓	✓	✓		1.095
K5-309	Outer	CICOREL		✓			1.113
K5-310	Outer	CICOREL	✓	✓	✓		1.095
K5-312	Outer	CICOREL	✓	✓	✓		1.113
K5-400	Outer	DYCONEX		✓		✓	1.171
K5-402	Outer	DYCONEX		✓		✓	1.171
K5-304	Inner	CICOREL		✓	✓		1.171
K5-307	Inner	CICOREL	✓	✓			1.150
K5-313	Inner	CICOREL	✓	✓			1.095
K5-314	Inner	CICOREL		✓			1.150
K5-316	Inner	CICOREL		✓			1.150

Table 1. SCT Forward electrical modules.

In all the measurements the ASICs are powered with the prototype SCT low voltage power supply, SCTLV3, and readout electrically via an SCT CLOAC-MuSTARD-SLOG system [4]. The sensors are biased with the companion prototype high voltage units (SCTHV).

The amplitude of the calibration pulse issued by the ASICs needs a correction factor, referred in the following sections as the calibration factor, that takes into account variations from the design value of the calibration

capacitor on the front-end. The correction factors are measured during the chip production testing on a wafer by wafer basis. These values are also compiled in Table 1.

Six of the modules have been irradiated with the 24 GeV proton beam of the CERN PS using the SCT irradiation facility [5]. The modules have been irradiated up to a fluence of 3×10^{14} protons/cm^2. Half of them, K5-305, K5-308 and K5-307 where irradiated in May 2002, while the other three in June 2002. One of them, K5-307, was used for thermal studies and was not tested electrically.

4 Results from individual modules.

The characterization of a single module has to demonstrate its functionality, that the performance of the ASICs does not degrade when assembled into the module, a stable performance of the module and that the specifications are met. To this end, front-end parameters, like the gain, output noise, offset spread and timewalk need to be measured and it should be verified that their values are uniform across single chips, as specified for the ASICs.

4.1 Gain, noise and noise occupancy.

For non-irradiated modules, the measurements have been made with a temperature on the hybrid thermistor of about 35-40 ºC. In order to compare the noise figures of the different modules, they have been normalized to the operating temperature of the SCT, which is 2 ºC on the hybrid thermistor. The noise slope versus thermistor temperature, after applying the calibration factor, has been measured to be 5.5 e$^-$ ENC/ºC for non-irradiated modules. Both the thermistor temperature and the slope are not very precise measurements and the expected accuracy on the noise figures is about 50 e$^-$ ENC. The validity of the temperature correction has been checked by measuring the noise of two of the modules at 2 ºC on the hybrid thermistor and the value obtained agrees with the corrected value within less than 40 e$^-$ ENC. For irradiated modules the slope is 15 e$^-$ ENC/ºC.

At the SCT temperature, the noise in all the modules has an average of about 1440 e$^-$ ENC for the outer modules, 1345 e$^-$ ENC for the middle modules and 920 e$^-$ ENC for the inner modules, as illustrated in Figure 1, where the average equivalent noise charge, in electrons, is shown for each of the 12 ASICs in all the modules tested. Table 2 shows the average noise values as measured, together with the temperature of the measurement for each unirradiated module. The value corrected by the calibration factor and temperature is also shown in the table

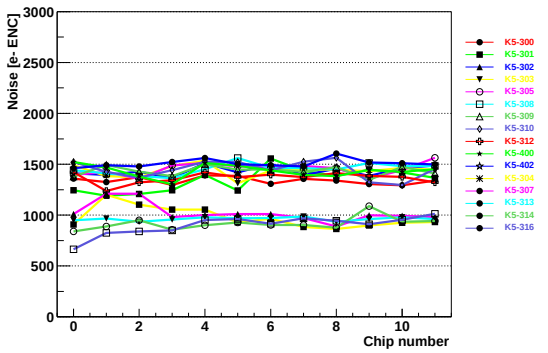


Figure 1. Measured noise (e$^-$ ENC) on each of the 12 ASICs of all the modules tested. The values are corrected by the calibration factor and normalized to 2 ºC.

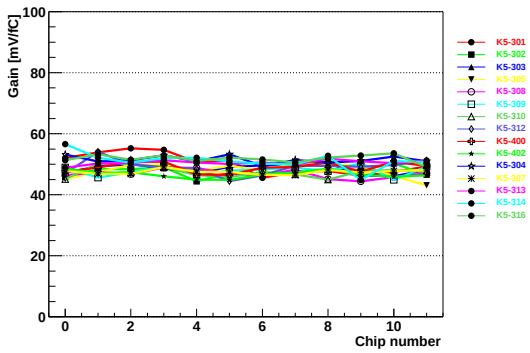


Figure 2. Average gain on each of the 12 ASICs of the modules. Values have been corrected with the calibration factor.

Figure 2 shows a similar plot for the average gain on each of the 12 ASICs of the modules. The average module gain is 48.9 mV/fC. The average value of the gain for each module is listed in Table 2.

Figure 3 shows example plots of occupancy versus threshold for all individual channels from the first readout side of an outer module. The smoothness and regularity of the curves are a very sensitive test of the intrinsic stability of the module.

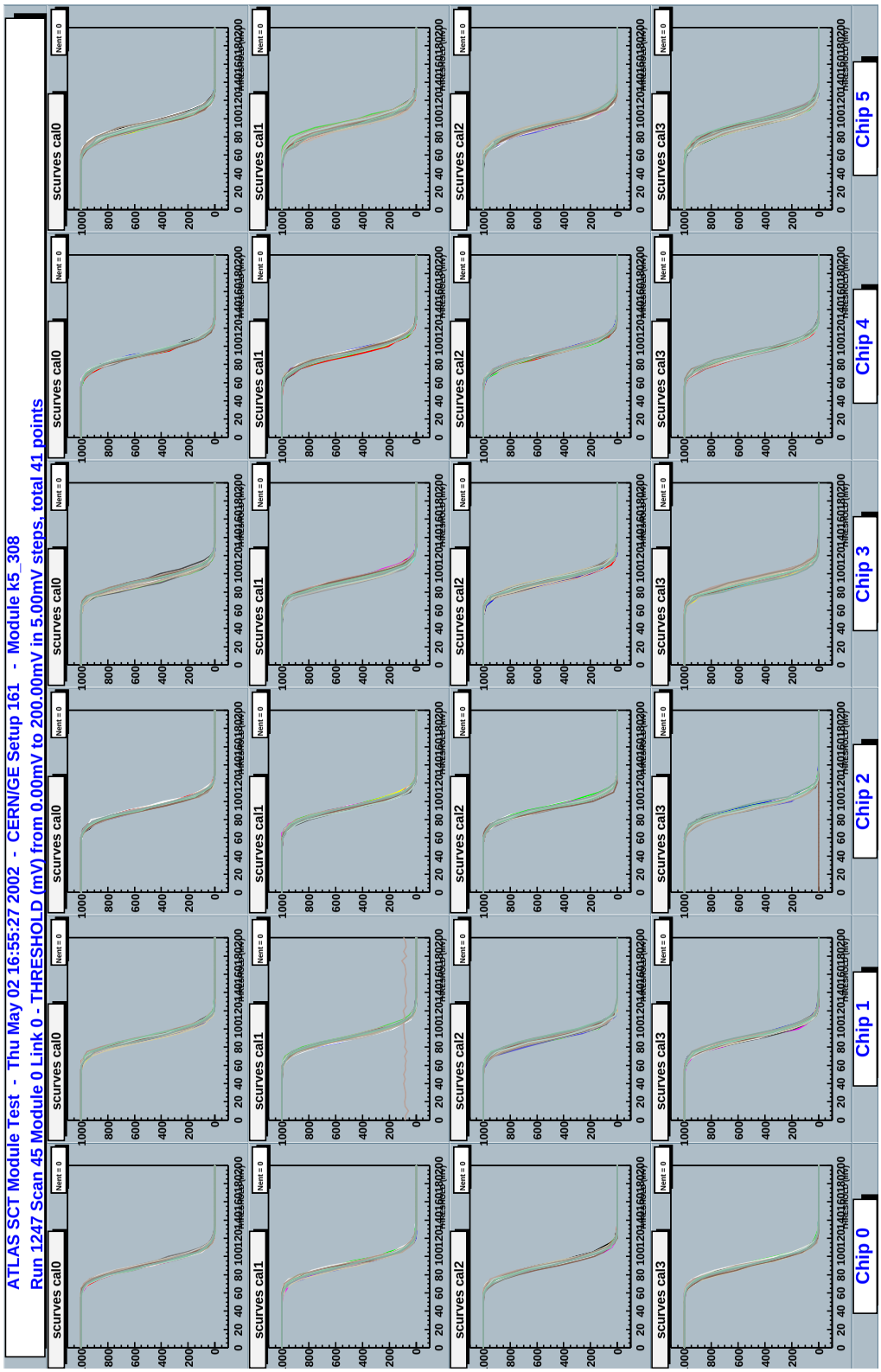


Figure 3. Curves of occupancy versus threshold superimposed for every readout channel of the first readout side of an outer module. Every fourth channel (32 in total) of each ASIC appears in each of the boxes.

The SCT design goal is to set the ASICs binary readout threshold at 1 fC, to ensure the high tracking efficiency for particles traversing the silicon at inclined angles, depositing charge on more than one readout strip. The measured noise occupancy of the individual unirradiated modules at this threshold is listed in Table 2. The table also shows the noise occupancy corrected by the calibration factor and the temperature. At the SCT

temperature, the average noise occupancy at 1 fC is ~10^{-5} for the outer modules, ~5×10^{-6} for the middle modules and smaller than 10^{-8} for the inner modules.

For the non-irradiated modules, the electronics noise is below the expected 1500 e^- ENC and the noise occupancy at 1 fC is well below the 5×10^{-4} level.

Module	*Type*	*Cal. Factor*	*Gain (mV/fC)*	*Thrs. Spread @ 1 fC (e^- ENC)*	*Temp. (°C)*	*Noise (e^- ENC)*		*Noise Occupancy @ 1fC*		*Masked channels*
						Meas.	*Corr.*	*Meas.*	*Corr.*	
K5-300	M	1.093	47.8	167	38.0	1407	1340	1.28E-05	5.74E-06	0
K5-301	M	1.093	50.1	160	40.0	1421	1351	1.50E-05	5.62E-06	10
K5-302	O	1.150	47.5	188	38.0	1419	1433	7.79E-06	9.99E-06	4
K5-303	O	1.171	48.5	168	33.0	1382	1442	6.50E-06	1.67E-05	8
K5-305	O	1.171	48.1	193	35.0	1393	1426	1.49E-05	3.62E-05	0
K5-308	O	1.095	46.8	183	47.0	1552	1449	4.83E-05	1.53E-05	4
K5-309	O	1.113	47.9	160	33.0	1435	1388	4.00E-06	3.37E-06	12
K5-310	O	1.095	47.4	140	40.0	1514	1449	1.66E-05	6.36E-06	0
K5-312	O	1.113	49.0	228	46.0	1524	1454	6.14E-06	5.93E-06	10
K5-400	O	1.171	49.0	160	33.0	1370	1434	2.09E-06	5.23E-06	3
K5-402	O	1.171	46.7	143	46.0	1484	1501	2.03E-05	2.45E-05	4
K5-304	I	1.171	51.5	118	43.5	1204	937	< 1.0E-07	<2.0E-08	1
K5-307	I	1.150	47.5	127	48.2	1276	984	< 1.0E-07	<2.0E-08	16
K5-313	I	1.095	50.5	150	43.5	1190	940	< 1.0E-07	<1.0E-09	10
K5-314	I	1.150	51.1	124	41.4	1134	885	< 1.0E-07	<9.0E-09	4
K5-316	I	1.150	51.8	142	41.9	1119	867	< 1.0E-07	<8.5E-09	4

Table 2. Front-end parameters as measured for the non-irradiated prototype end-cap modules. The values are corrected for the ABCD calibration capacitance variation where needed. For the noise and noise occupancy, the column labeled as Meas. shows the measured value and the column labeled as Corr. the value corrected and normalised to the SCT operating temperature.

Table 3 summarizes the front-end parameters of the irradiated modules. They have been measured with temperatures on the hybrid around 1 °C. K5-305 and K5-308, irradiated during the May 2002 period, show a higher noise (>2100 e^- ENC) and threshold spread (~600 e^- ENC), together with a smaller gain than the modules irradiated in the June 2002 period, which have a threshold spread of ~500 e^- ENC, and a gain value within the expectation. The contribution of noise and threshold spread yields, however, a noise occupancy at 1 fC of ~10^{-3}, above the 5×10^{-4} level. Nevertheless, the nominal noise occupancy would be reached, both in K5-310 and K5-312, with a threshold of 1.09 and 1.06 fC. The higher threshold spread and electronics noise of K5-305 and K5-308 could be explained by a higher dose compared to the June 2002 period. An increased dose would produce a bigger threshold offset and a higher β drop with, consequently, a higher noise.

Module	*Type*	*Gain (mV/fC)*	*Thrs. Spread @ 1 fC (e^- ENC)*	*Temp. (°C)*	*Noise (e^- ENC)*		*Noise Occupancy @ 1fC*	
					Meas.	*Corr.*	*Meas.*	*Corr.*
K5-305	O	27.6	614	1.0	2052	2408	5.48E-03	8.80E-03
K5-308	O	32.2	573	1.0	1990	2185	2.11E-03	4.40E-03
K5-310	O	33.8	490	8.0	1843	2068	4.18E-04	1.27E-03
K5-312	O	37.7	534	-1.0	1717	1928	3.31E-04	1.05E-03

Table 3. Front-end parameters as measured for the irradiated prototype end-cap modules.

4.2 Threshold and gain uniformity.

For the binary architecture, one of the most critical issues is the uniformity of the parameters of the front-end circuit and, especially, matching of the discriminator threshold and the gain. In order to minimize the impact of the threshold non-uniformity on the noise occupancy, the ABCD3T implements an individual threshold correction in every channel using a 4-bit DAC (trim DAC) per channel with four selectable ranges. One can, therefore, minimize the threshold spread in the chip at the operating threshold.

Figures 4 and 5 show the threshold spread, for the non-irradiated and irradiated modules, respectively, after trimming the threshold at 1 fC for all the channels. The unirradiated modules have an average threshold spread of 160 e^- ENC. This is to be added in quadrature with the electronics noise to obtain the effective noise that will produce the measured noise occupancy. For the irradiated modules the matching of the discriminators degrades and, therefore, a wider range of the trim DAC is needed to reduce the threshold spread. With this range, the average spread is 590 e^- ENC. Tables 2 and 3 show the average threshold spread for each module.

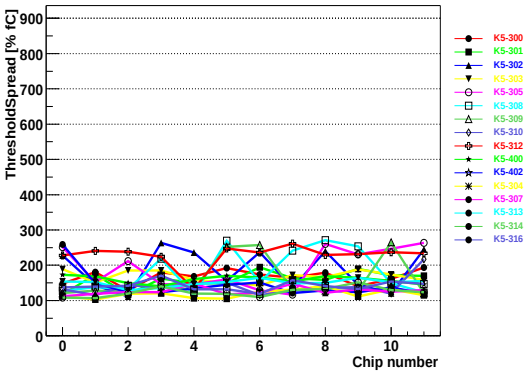


Figure 4. Average threshold spread, in e^- ENC, on each of the 12 ASICs of the non-irradiated modules.

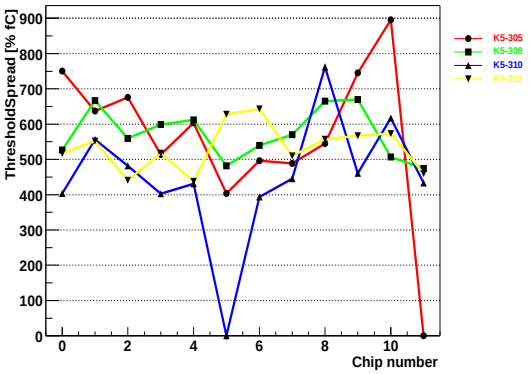


Figure 5. Average threshold spread, in e^- ENC, on each of the 12 ASICs of the irradiated modules .

4.3 Power consumption.

The power consumption at 1 fC threshold, for both irradiated and unirradiated modules, has an average of 5.5 W as measured during the noise occupancy scans, with a trigger frequency of 100kHz. The maximum value is 6.5 W, at the highest occupancy. This also includes the currents drawn by the opto-chips and the hybrid itself.

4.4 Timewalk.

In order to ensure a proper beam crossing identification and to reduce the inefficiency produced by the assignment of hits to the wrong time slot, the time-walk should be smaller than 16 ns [1,2]. Here the time-walk is defined as the maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC. Figure 6 illustrates the procedure for a non-irradiated modules (a,b) and an irradiated module (c,d). Figures 6b and 6d show the efficiency curve versus the delay in DAC units between the trigger and the clock edge. The width should be 25 ns and its value in DAC units is related with the speed of the digital part of the ABCD3T (the higher the faster). It can be seen that after irradiation the digital block is slightly slower.

Figures 6a and 6c show the variation of the delay for the efficiency plateau with increasing input charges. Smaller DAC values correspond to the plateau being reached later. The difference between the delay at 1.25 and 10 fC input charge gives the time-walk of the comparator. Non-irradiated modules have, typically, a time-walk of the order of 10 ns, while the irradiated modules have about 13 ns. This corresponds to a peaking time of the order of 22 ns and 30 ns respectively.

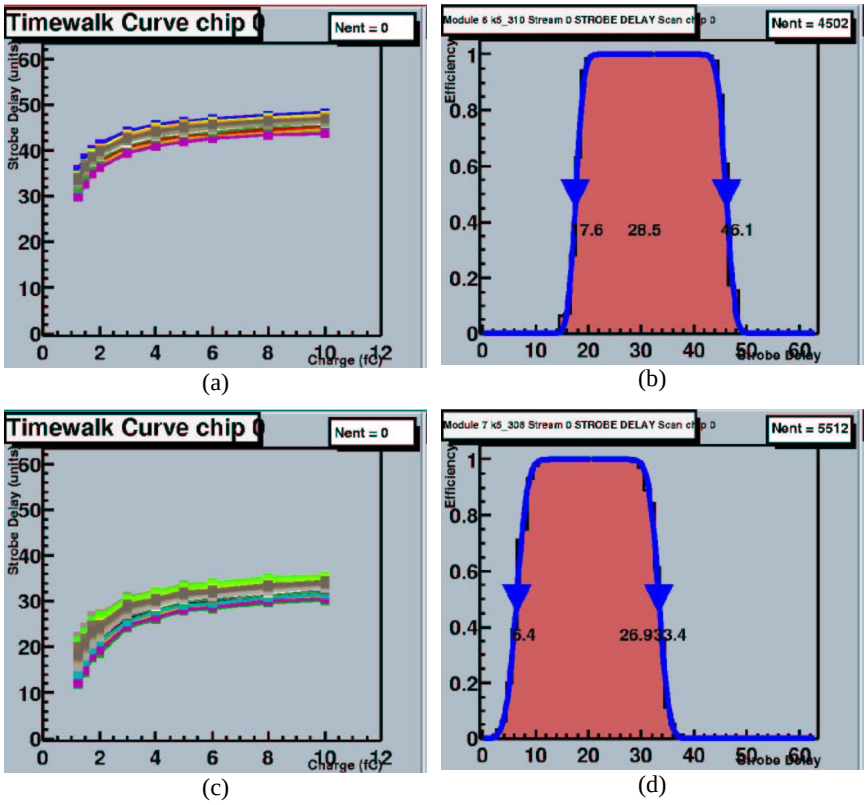


Figure 6. (left) Timewalk curves for all the channels in a chip of a non-irradiated module (a) and on an irradiated module (c). The difference between the highest and lowest point in the curve gives the timewalk in DAC units. To convert DAC units to ns, the efficiency curves versus DAQ delay are used, as shown on the right figures (b non-irradiated, c irradiated). The with of the plateau should be 25 ns. The conversion factor is related to the speed of the digital part of the chip.

4.5 *Bit-Error-Rate testing of opto-links.*

The Bit-Error-Rate (BER) for the SCT opto-links has been studied with a K5 hybrid, populated with DORIC4A and VDC chips [6]. A plug-in opto was used for the data and Timing, Trigger and Control (TTC) links.

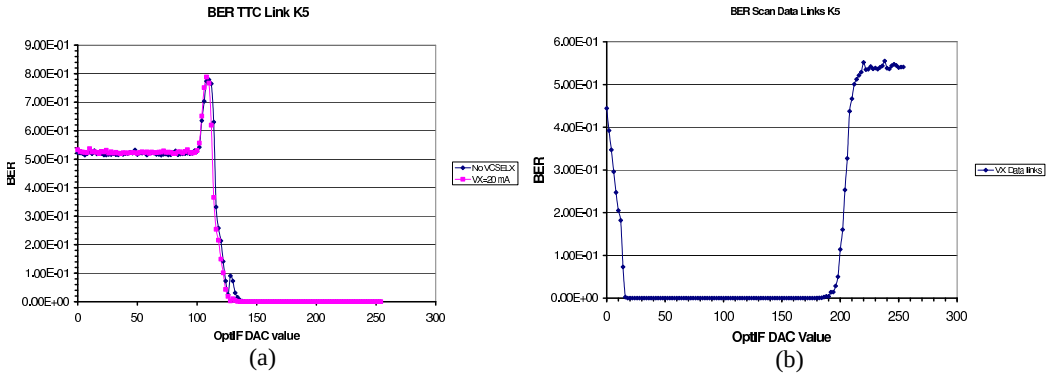


Figure 7. BER scans for the TTC (left) and data (right) links.

There is no evidence of cross-talk between the data and TTC links and the 90%CL upper limit for the BER on the TTC link is 1.9×10^{-11}. The measurements were done obtaining the BER as a function of the optical power of the VCSEL in the readout crate. The results are shown in Figure 7a. As for the data links, Figure 7b shows the variation of BER as a function of the receiver threshold on the readout crate. The 90% CL upper limit for the BER on the data link is 1.6×10^{-10}, which is well below the specification of 10^{-9}. Further tests should be performed on a K5 fully loaded with ABCDs.

5 System test and first results.

5.1 General Description

The system test simulates a section of one of the SCT forward disks in all its details of mounting, cooling, supply and shielding. Details on the sector prototype can be found in [7].

The sector can accommodate up to 33 modules; 13 outer, 10 inner and 10 middle modules. Figure 8 shows the outer and inner module mounting positions on the front of the disk; Figure 9 shows the back of the disk where the middle modules are mounted. The mounting positions are denoted O1-O13 for outer and I1-I10 for inner positions starting at the far left of Figure 8. The middle positions are denoted M1-M10, counting from the right of Figure 9. Figure 10 shows the sector with four outer modules assembled.

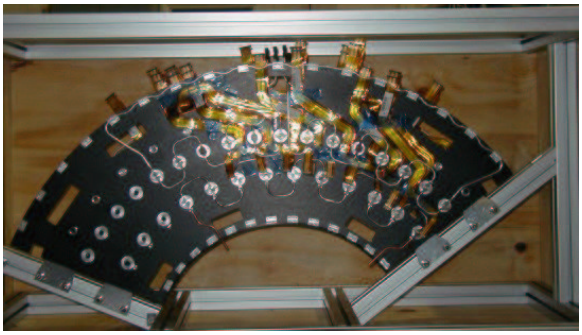


Figure 8. Sector Front view.

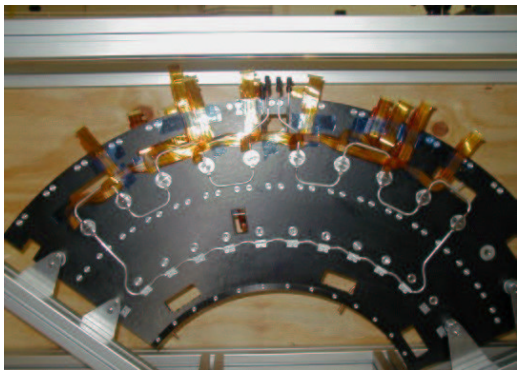


Figure 9. Sector Back view

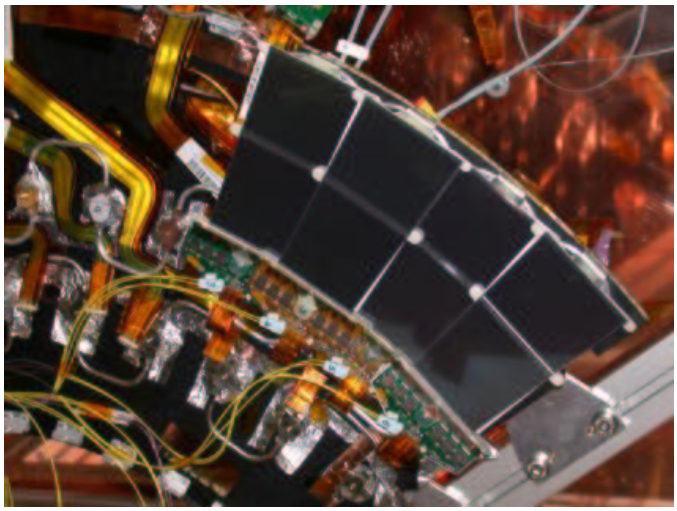


Figure 10. View of the sector with 4 modules assembled.

The disk is held at each end via metal bolts to an aluminium support frame, shown in Figures 8 and 9. The carbon-fibre disk is therefore in electrical contact with the support frame. The sector is housed in a copper box to represent the thermal shield at the SCT. It should be noted that the cover is not electrically or geometrically similar to the planned ATLAS SCT thermal shield. Combined with blackout cloth and a dry nitrogen supply the copper box provides a dry and dark atmosphere, with a relative humidity of 20% or less, whilst running.

Separate cooling circuits are used for the three module types. The inner modules are served via a CuNi pipe 4mm OD with 70µm wall thickness, while the middle and outer modules have aluminium pipes 3.6mm ID/ 4.0mm OD. The cooling blocks are machined Al blocks with copper plating at the pipe block join. The blocks were soft soldered to the cooling pipe. On the outer cooling circuit 4 of the high cooling blocks are carbon-carbon with a Cu plate (positions O3, O5, O7 and O9). The third carbon-carbon block had a final gold flash to prevent oxidation. An ethanol-water mixture is pumped through the pipes; a commercial chiller controls the temperature of this cooling mixture.

The low mass kapton power tapes (*wiggly* tapes) were produced at Ljubljana. They were made from the *old* design, with Al tracks and withs varying from 21 mm at the outer diameter of the disk, narrowing to 14 mm at the module. Because of the expense of producing different shapes of tape, only 9 different designs were

produced. Therefore 9 positions have the correct tape layout and the remaining positions have tapes which have been *made to fit* as well as possible. The wiggly tapes contain the power, select, reset and temperature monitor lines for the modules. The communication of clock, commands and data to and from the module is performed via the optical plug-ins in the forward optical harness. Each harness serves either 5 or 6 modules. At the edge of the disk the harness connects to 25 m long fibres, which transmit the data to the DAQ system, illustrated in Figure 11.

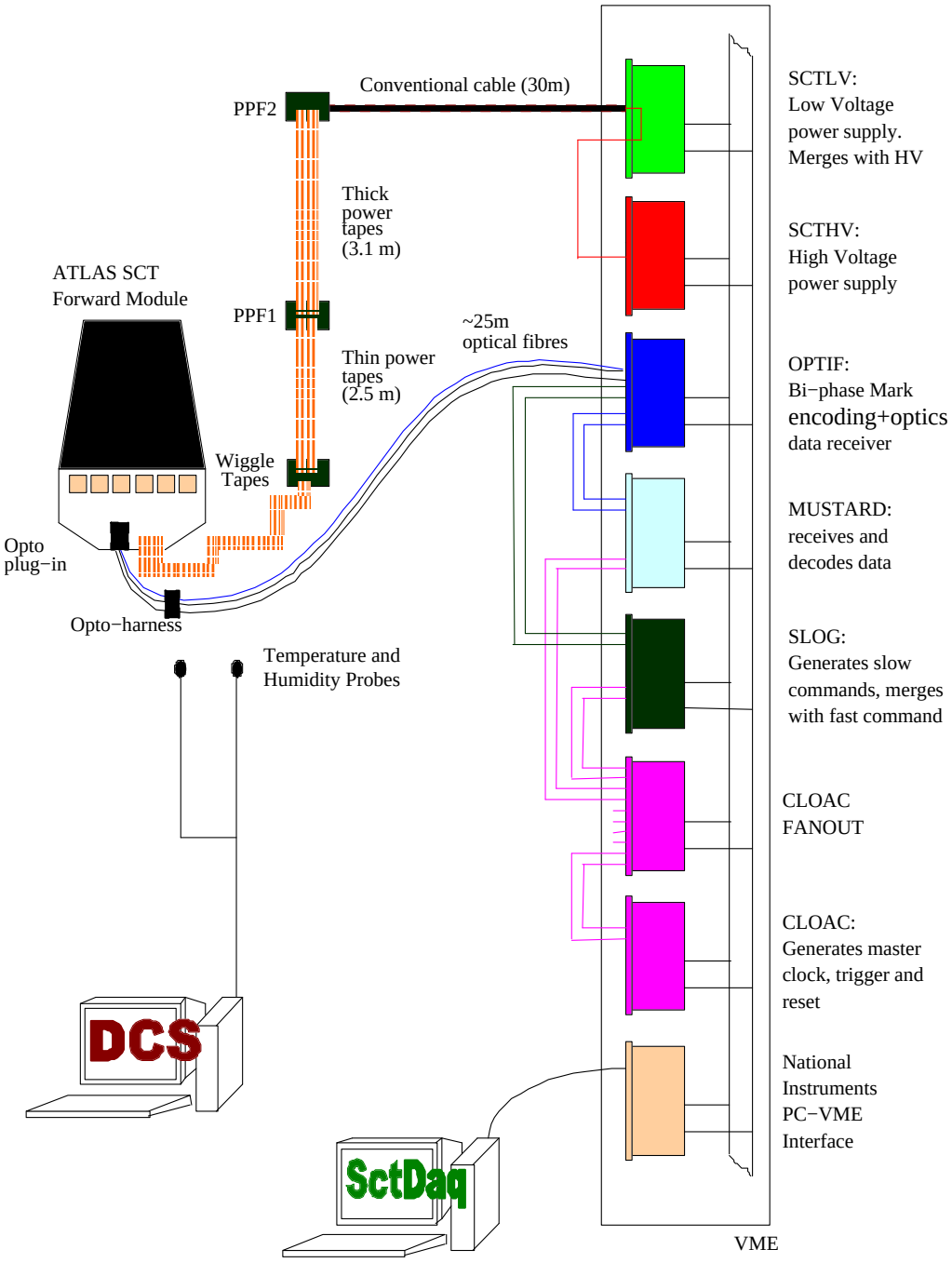


Figure 11. A schematic layout of the forward SCT system test.

The SCT prototype VME power supplies (SCTLV3s) power the module's ASICs and opto-components. The detectors are biased with the companion prototype high voltage units (SCTHVs). The individual channels of each power supply are floating with respect to each other. It should be noted that the return lines of the ASIC analogue and digital lines and the detector bias line are connected together at the disk in a fashion dependent on the particular grounding and shielding scheme implemented, which are described later.

The modules are read out using a CLOAC-SLOG-MuSTARD-OPTIF system, with the OPTIF [4] providing the electrical-optical interface. The DAQ used is in place of the final read-out drivers, (ROD). The hybrid temperature is readout via the SCTLV3 modules. A ROOT-based SCTDAQ software package is used, running on a Windows-NT PC connected to the VME crates via a National Instruments interface card.

Control and monitoring of all voltages and currents is carried out through the DAQ software, although a prototype DCS system is used to monitor hybrid temperature, environmental temperature and humidity and control the cooling unit.

All patch panels used are as close as possible to the planned final ATLAS design, except for extra provisions to allow testing of various coupling schemes. From the power supplies 30 m long conventional cables run to PPF2 via a common mode choke. These chokes are intended for use at PPF3 but PPF3 is not represented in the system test. Between PPF2 and PPF1 2.5 m long kapton tapes with 100µm thick Al tracks are used. The kapton tapes between PPF1 and PPF0 are 3. m long with 50µm thick Al tracks. A schematic diagram of the system test is shown in Figure 11.

5.2 Grounding and Shielding in the System Test

The system test bases it's grounding and shielding scheme on the proposal outlined in [8,9,10]. These differ in the way the modules are referenced with respect to each other. The main elements as applied in the system test are described below, with any differences noted. Variations to this scheme are being investigated to seek improved performance. At the SCT low voltage power supply, the conventional cable shield is AC connected via a 10 nF capacitor to digital ground.

At PPF2, the conventional cable shields pass through the chokes and are commoned at the kapton-tape side of PPF2. From PPF2 to PPF1 the 6 *thick* kapton tapes per PPF2 are bundled together and wrapped with aluminium foil. At PPF2 the shield is connected, via jumpers, to the aluminium foil wrapped around the kapton tapes and taken to PPF1. PPF1 is electrically shielded inside an aluminium box, connected to the kapton aluminium foil shield. PPF1 is equipped with jumpers to allow AC connections of all lines to the shield. VCC and VDD are AC coupled to their respective return lines via 4.7 µF capacitors. HV and HV return are AC coupled with a 10 nF capacitor. All power and return lines (including Pin bias and VCSEL lines), sense lines and the select line are AC coupled to the shield via 1 µF capacitors. No connection (AC or DC) is made between the HV and the HV return lines to the shield at PPF1. From PPF1 to PPF0 the *thin* kapton tapes are bundled together in sets of 3, with each set wrapped in aluminium foil. The shield connection continues via the aluminium foil around the *thin* kapton tapes through the sector housing to PPF0. The shield is held in good electrical contact with the copper box at the entry point. The disk's aluminium support structure, inside the copper box, is electrically connected to the disk's carbon fibre skin via copper tape and via supporting screws into the structure of the disk.

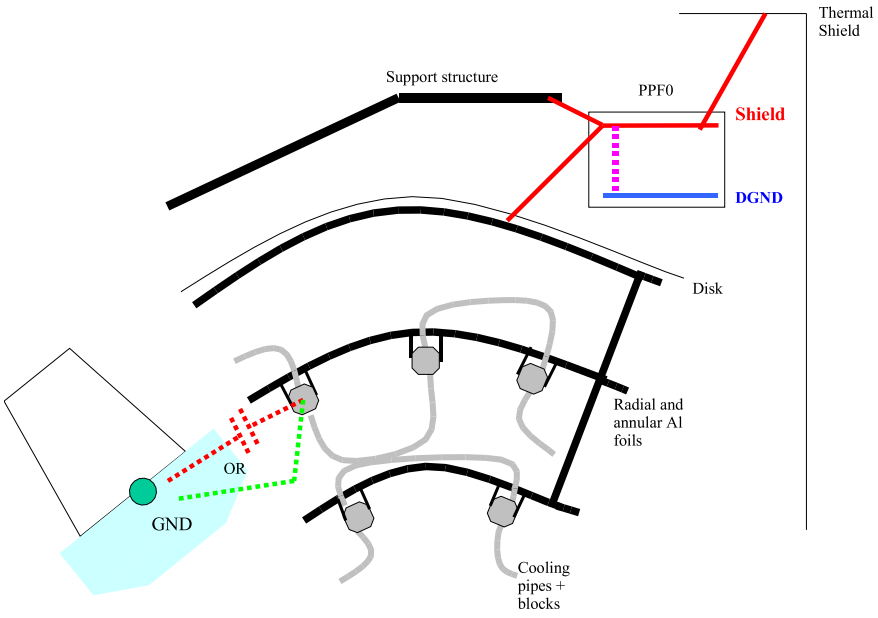


Figure 12. Detail of on disk and PPF0 grounding and shielding scheme.

The shield at PPF0 is connected to a 50μm thick annular Al foil ring, one on each face of the disk at the outer radius. These rings are connected together and to the carbon fibre of the disk with conductive epoxy and copper tape. On each disk face the annular foil is connected via three radial foils to annular foils running just above the cooling blocks, (2 foils on the disk front and 1 on the back), that have foil tabs connected to each cooling block. Connections are made between the foil and the cooling block using either conductive epoxy or the cooling block's fixing screws. In this manner all the cooling blocks are connected, via Al foil, to the outer annular foil and thus the shield at PPF0. At PPF0 the shield is connected to DGND, via jumpers fitted to PPF0. The shield at PPF0 is also connected to the aluminium support structure via short pieces of copper tape.

The prototype K5 modules used in the system test have an integrated shunt shield at the module mounting point. This is shorted so that the module power returns are DC connected to the cooling block at the module mounting point. A schematic representation of the on-disk-grounding scheme is shown in Figure 12.

Figure 13 illustrates the main features of the grounding and shielding scheme. The red dotted line represents the shield; while only the VDD and DGND lines are shown in reality both analogue and digital lines pass through a choke and are AC coupled to the shield at PPF1.

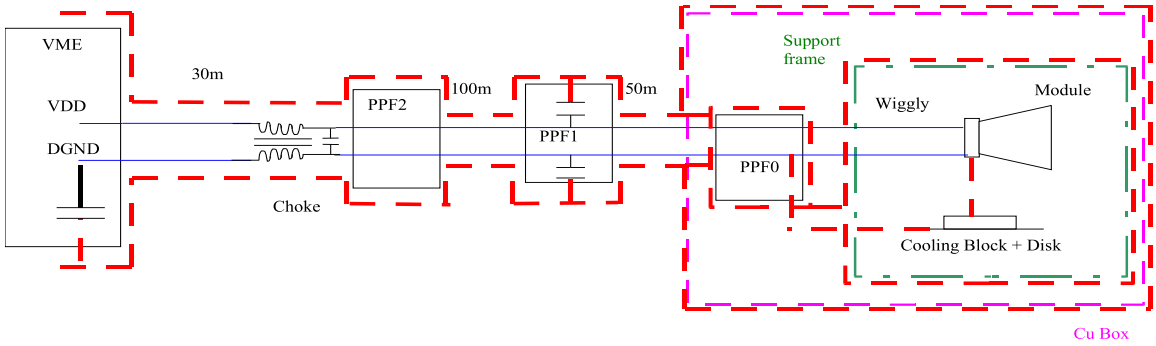


Figure 13. Grounding and shielding scheme that utilises DC connection between the AGND of each module and its cooling block, and a DC connection between shield and DGND at PPF0.

Variations to the grounding and shielding scheme include the use of a shunt shield between the module AGND and the cooling block, implemented at the cooling block. The module ground and the cooling block are not in intimate electrical contact with each other. The shield connection at PPF0 to DGND is maintained. Thus the cooling circuit is connected to the modules digital return via a long path consisting of the wiggly tapes and PPF0. At PPF1 the HV line is AC coupled to the shield via a 10nF capacitor and the HV return line is shorted to the shield.

The second variation requires the module grounds to be held together as tightly as possible and referenced to the cooling circuit. The DC connection between shield and DGND at PPF0 is removed, resulting in a single connection of module ground to shield via the cooling circuit.

All the variations of the ground and shielding schemes investigated gave equally good performance for the system in the absence of artificially generated noise sources; the results are discussed in section 3. Section 4 reports on the first measurements made with an artificial noise source injected into the system.

5.3 First results for the Forward system test.

When a module arrives at the system test it is verified to be in good working order, and mounted on the system test sector. A standard characterisation sequence is performed powering only that one module. Its performance is compared to the results from the module's construction site and any differences are noted and investigated if possible. The module is now considered ready to be included in multi-module tests.

So far, six modules (two middle and four outer modules) have been used in the system test; detailed in Table 1. All the modules showed approximately the same noise values (within about 100 ENC) when running alone on the sector as they did on the bench.

A typical multi-module test is to measure the gain, noise and noise occupancy with many modules running in parallel. This has been performed, using a three-point gain calculation and noise occupancy scans, with the modules on the sector. At present either the two middle modules or the four outer modules have been operated together, but not all six at once. For example the 4 outer modules were mounted in positions O10 to O13 (O11

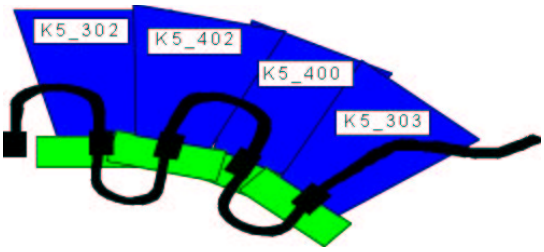


Figure 14. modules & cooling pipes in a 4 outer multi-module run

and O13 being high blocks) as shown in Figure 14. The modules were communicated with via a single opto-harness. Details are given in Table 4.

Module	***Cooling block***	***Opto plug-in***	***Temperature (°C)***
K5-302	O10	3	34
K5-402	O11	4	37
K5-400	O12	5	35
K5-303	O13	6 (only link1 working)†	37

Table 4. Multimodule tests on 4 outer modules.
†All 12 ABCDs were read using a single link.

The measured noise values of the ASICs on the modules, with either all 4 outer modules or the 2 middle modules operating together are shown in Figures 15a and 15b. The input noise was corrected for the correct calibrate capacitor value and for a hybrid temperature of 2C. The input noise is consistent with the values obtained when the modules were electrically readout in a test-box.

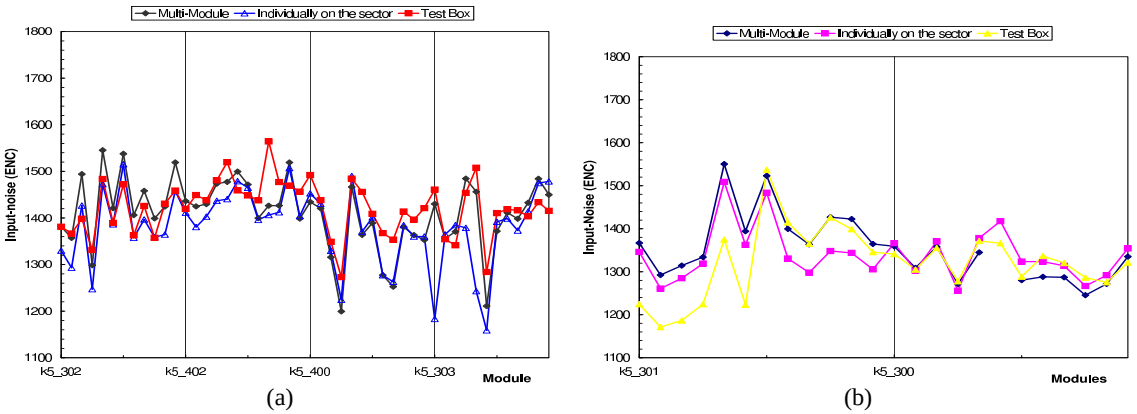


Figure 15. Comparison of the measured noise (e^- ENC) of each ASIC per module measured on the system test sector when the modules were operated individually and as part of a multi-module run and with electrical readout in a test box: (a) outer modules (b) middle modules.

A scan of noise occupancy as a function of threshold was performed; illustrated in Figure 16 for one module. Good agreement in the noise measured by the 3point gain and the noise occupancy runs were obtained. Figure 17 shows the noise occupancy measured for the 4 outer modules when operated individually and together on the sector and in a test-box. It should be noted that this data does not include the calibrate capacitor correction value, except for the test-box data of module k5_402. The noise occupation was within specification with a measured value below $5x10^{-4}$.

Noise occupancy as a function of time was measured with the threshold set to 1fC on all modules. The duration of a noise occupancy measurement was about 1 minute, with a 2 minute interval been measurements. 100 measurements were made. Figure 18 shows the observed decrease in noise of one module as a function of time. This effect, which has also been observed in barrel modules, has been attributed to the change in the inter-strip capacitance of the detector as a function of time after the initial bias is applied to the device. The time constants are detector dependent and for some modules can be as long as an hour. This imposes no implications on the running of the SCT. However, the system test has to be left biased for at least an hour for comparative studies of

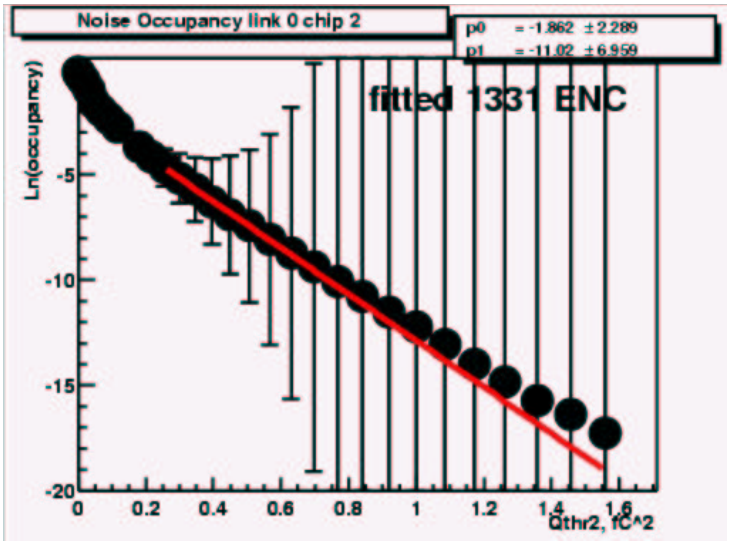


Figure 16. An example of ln(Noise Occupancy) as a function of threshold squared (fC^2) measured in a multi-module run

noise performance. There were no peaks detected in the noise occupancy versus time plots. Had peaks been present this would be indicative of inadequate shielding.

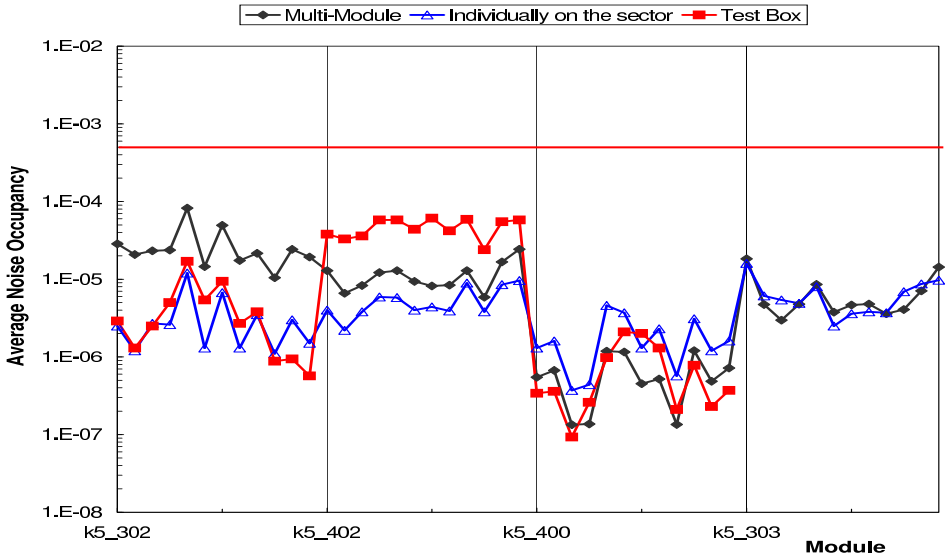


Figure 17. Comparison of the noise occupancy per chip measured with all 4 outer modules operated together on the sector, individually on the sector on in a test box. The red line indicates the limit imposed by the specifications.

An initial run of a correlated noise data taking macro for the 4 outer modules with one million triggers and a 0.8fC threshold was taken. This resulted in a low number of events and therefore large statistical uncertainties in the value of the correlated noise. However, the noise calculated from the correlated noise measurement agreed with those from the 3pt gain scan, while the amount of correlated noise found was low and consistent with zero.

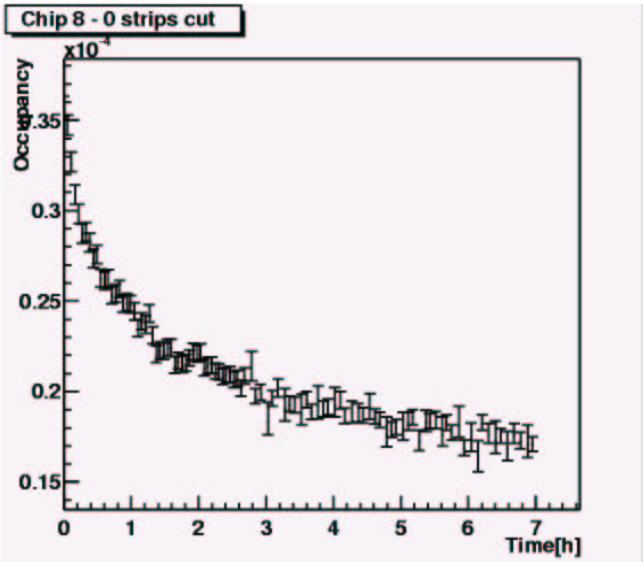


Figure 18. Noise Occupancy as a function of time.

5.4 Noise injection studies with shunt shield grounding option

Experiments are ongoing to investigate the robustness of the grounding and shielding against injected noise. Noise is injected either into the cooling pipes on the disk or the thick power tapes (between PPF2 and PPF1) with the use of ferrite rings to induce an AC current into the system. The ring was placed around the tapes between PPF2 and PPF1 or around a cable connected to the cooling pipes outside the copper enclosure. Both the magnitude and frequency of the injected signal were altered and the effects noted.

Single threshold scans with a 2fC injected charge pulse were taken. The noise was obtained on a strip-by-strip basis from the threshold scan s-curves. Assuming a fixed gain of 55mV/fC the noise as ENC in electrons was determined. The average noise per chip was then computed. Each set of measurements was comparative in nature and therefore a reference set of data was taken without noise injection followed by the measurements with the noise source. The difference between the two sets was plotted.

Figures 19 and 20 illustrate the dependence on the noise pick-up as a function of frequency, for injection into the tapes and the cooling pipes, respectively. A strong peak in sensitivity between 6-10MHz was observed, as expected from the front-end band-pass characteristics. Increasing the magnitude increased the injected signal size, which is shown in Figure 21 for an 8 MHz AC noise signal injected into the kapton tapes.

The structure in the noise is module position dependent and it is greater where the modules overlap each other and overlap the cooling pipes, and power tapes. Module k5_402, which is in a lower module position, shows increased sensitivity to noise pick-up probably due to its closer proximity to the cooling pipes and power tapes. A difference in the amplitude and distribution of the excess noise is observed between the tape and pipe injection methods. Noise rejection was observed to be better with the default grounding option compared to the two variations described above.

It should be noted that these measurements are very preliminary and on going. Further improvements in the grounding and shielding schemes are continuing to yield improvements in noise rejection and further study is on going.

In conclusion the system test has shown that the modules are within specification when operated together (although in very limited numbers at present) without the deliberate injection of noise into the system. The noise injection studies have resulted in no conclusive answer to the exact ground and shielding scheme and, therefore, to the requirement or otherwise of shunt shield.

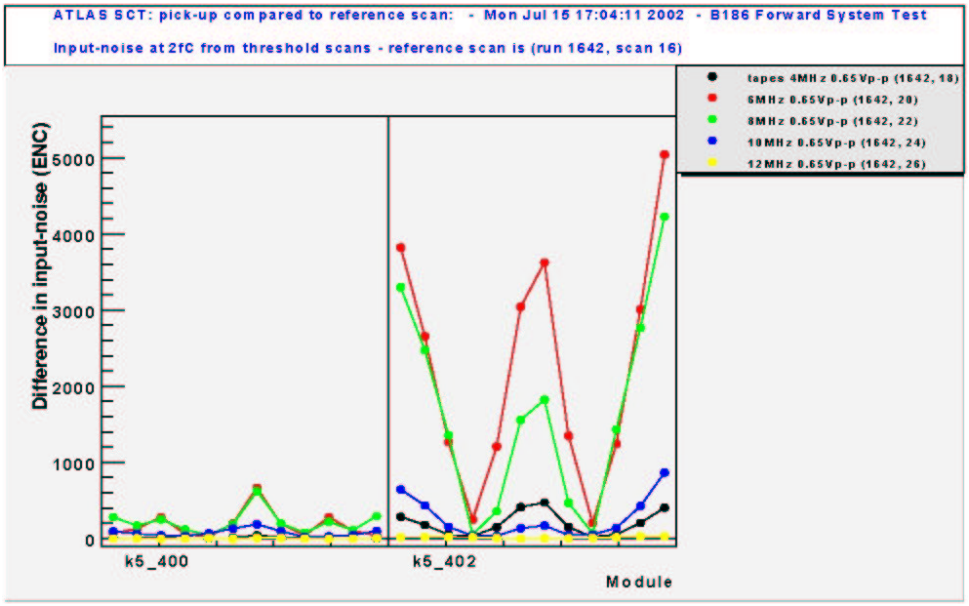


Figure 19. Excess input noise (e- ENC) due to noise injection into the kapton tapes, as a function of signal frequency.

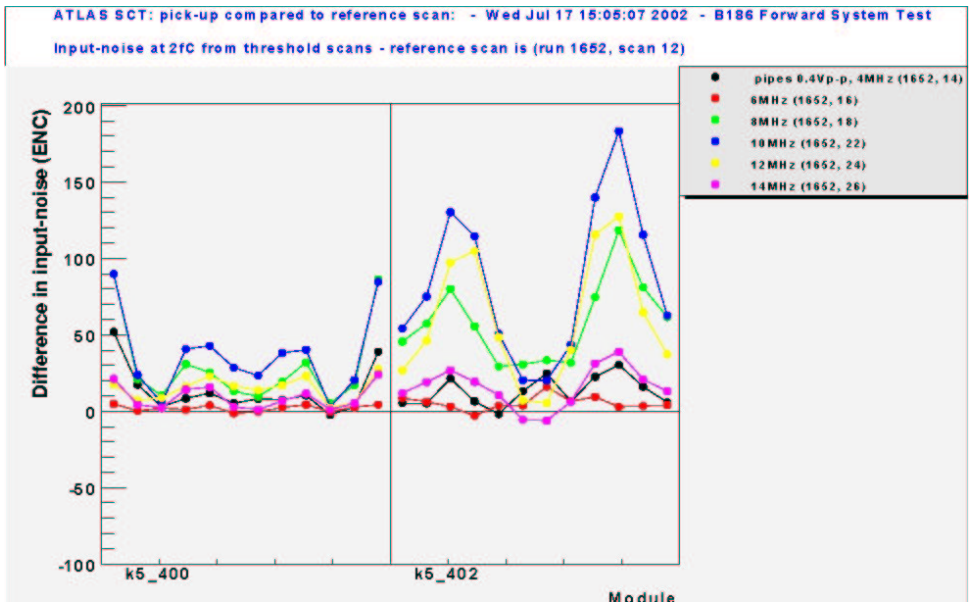


Figure 20. Excess input noise (e- ENC) due to noise injection into the cooling, as a function of signal frequency.

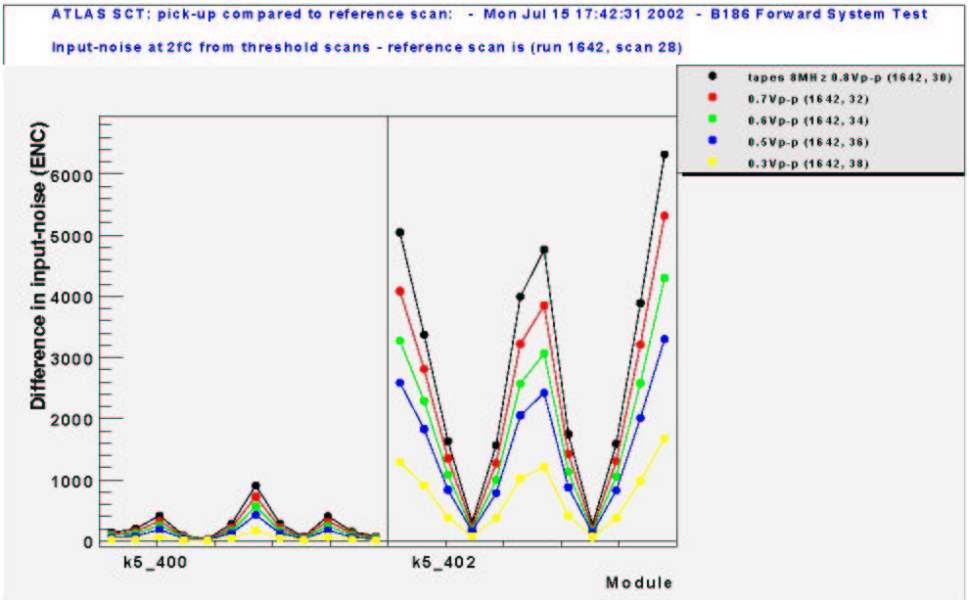


Figure 21. Excess input noise (e- ENC) due to an 8MHz AC noise signal injected into the kapton tapes, as a function of signal magnitude.

6 Module Test-Beam results.

6.1 Introduction.

Testbeam measurements have been performed to evaluate the tracking performance of a number of the prototype SCT end-cap modules. The measurement program was designed to investigate the response of individual modules to single high-energy particle tracks through a range of systematically varied operational and environmental parameters. These results may then be used to study the expected performance in ATLAS at much higher trigger rates and track densities. Two of the modules tested were those irradiated previously with 24 GeV/c protons at the CERN PS T7 facility to the SCT reference dose of 3×10^{14} p/cm^2. Related beamtests have been performed in previous years on barrel SCT modules (which have much in common with SCT forward modules, including basic detector technology and the same readout ASICs)[12,13], and prototype end-cap modules [12].

6.2 Facilities and setup.

The beamtests were performed at the ATLAS testbeam facility at the CERN SPS H8 beamline. A collimated, parallel beam of 180 GeV/c pions with some muons, about 1cm across, traveling in air, is passed through a pair of trigger scintillators and an inline array of silicon detectors as shown in Figure 22. The particle type and energy is chosen for negligible multiple scattering within the SCT setup while allowing adequate beam intensity. Beam intensity is set to around 20,000 particles per second for the duration of the SPS spill, 4.8 seconds in a 16.8 second cycle. Around 10 SCT modules-under-test are arranged one after the other, presenting approximately the same aspect to the incident beam. The modules are mounted on a rack which rotates each module about its own axis through a range of about $\pm15^{o}$ from normal, the whole array being always at the same angle to the beam. Each SCT module is contained in its own module box of a standard design incorporating liquid cooling to the main cooling block which is not split. In the case of the middle and outer modules, the end cooling block is also cooled by conduction through the aluminium frame. In the case of inner modules, the end block is thermally insulated. The boxes are covered by perspex sheets to present minimal material to the beam while enclosing each module in its own thermal environment. The modules and their associated mechanics are all contained within a larger thermal enclosure flushed with cold nitrogen gas. The liquid coolant and the gas are maintained between -10 and -20 ºC in order to keep the module temperatures low. The irradiated modules were cooled by dedicated chillers, measured at the hybrid thermistor to around +5 ºC on the irradiated modules in May/June, and -2 ºC in July after extra measures were taken. The unirradiated modules were somewhat warmer.

In addition to the 10 SCT modules, the SCT testbeam facility is equipped with four X-Y pairs of tracking detectors forming a silicon telescope. These are arranged in pairs immediately upstream and downstream of the

thermal enclosure. Their function is to provide high spatial resolution, ~3 μm, space points from which independent, high resolution tracks through the modules-under-test can be reconstructed.

To cope with the short shaping time of the ABCD3T chip and given that the SPS fixed target beam is not synchronous to the ABCD3T clock, the set-up is equipped with a 0.2 ns resolution TDC and an SCT CLOAC trigger synchronisation module. The CLOAC delays the propagation of external triggers both for the integer number of clock cycles required for the pipeline and for the fraction of a clock cycle required to synchronise the trigger with the internal latching of the discriminators. This fractional clock delay is measured by the TDC allowing offline selection of timing windows.

Data acquisition uses the standard SCTDAQ setup, including the SLOG, MuSTARD and CLOAC SCT VME modules and the ROOT software package, extended to handle synchronised triggers, event-by-event recording, and to read the telescope and TDC. Modules are electrically connected to the readout system using their spy connectors via the Melbourne patch and support cards rather than optical readout. Low and high voltage power supplies are also the standard SCT VME modules.

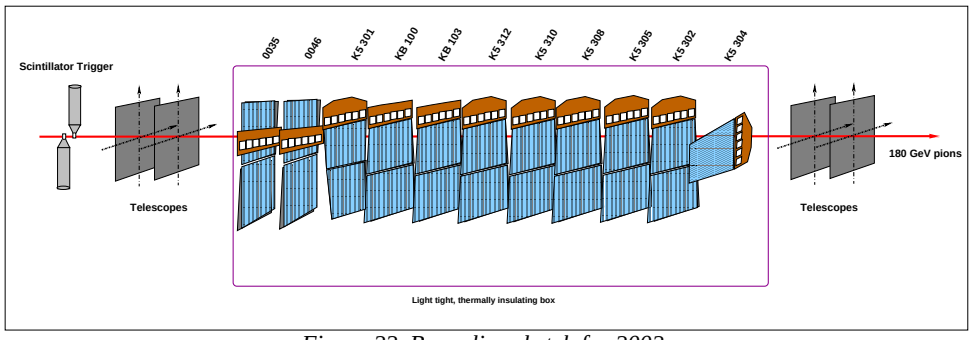


Figure 22. Beam line sketch for 2002.

The modules are calibrated using the internal calibration circuit of the ABCD chips immediately before the start of the test beam once the modules have stabilised at their operating temperatures and nominal bias voltages. In the case of the irradiated modules, a lengthy characterisation process to optimise the front-end settings after annealing and while at operating temperatures must be performed. Characterisation is repeated several times during the beamtest to check reproducibility, though in general the calibration constants are not changed unless clear errors are found. A number of bad channels identified during the calibration are masked online (so never resulting in hits), while a varying number of additional channels are masked during the offline analysis. The results presented below are based on an analysis of the remaining "good channels". The effect of masking on the overall efficiency is evaluated in Table 5. In all cases the efficiency loss due to masked channels is less than 1%.

module	***mask***	***Off-line mask***	***Efficiency loss (%)***
K5_304(I)	1	9	0.7
K5_301(M)	1	4	0.3
K5_302(O)	1	1	0.1
K5_310(O)	0	0	0
K5_312(O)	10	0	0.7
K5_305(irr O)	6	7	0.8
K5_308(irr O)	7	6	0.8

Table 5. Channels masked in hardware and software on all modules. The last column lists the resulting efficiency loss under the assumption that the tracks are uniformly distributed over the module.

The detector bias voltage of the irradiated modules was up to 450V in May/June, and up to 600V in July. In all cases the total leakage current was less than 3mA resulting in a voltage drop across the 11kΩ of the bias filter circuit of at most around 30V.

6.3 Measurement goals and Program.

The basic testbeam measurement of SCT binary modules is a scan of the input comparator thresholds resulting in s-curves of particle detection efficiency versus threshold. Several tens of thousands of randomly timed events are taken at each threshold point. Each event is analysed for matching telescope tracks and optimal timing efficiency to determine an efficiency. From these data, the efficiency around the design operating threshold, 1.0 fC, can be determined, as can the median charge response, defined as the threshold at 50% efficiency. Measurement of the median charge response allows an absolute calibration of the internal charge injection calibration circuits of the readout chips. By studying the same data as a function of timing window cuts, the pulse shape can also be mapped. Combining the median charge response with measures of the noise allows signal-to-noise ratios to be determined. Combining the experimentally determined charge scale with separate noise measurements allows a determination of the expected noise occupancy at operating thresholds along with a measure of the operating margin. Analysis of a large number of events at the operating threshold also allows a determination of the spatial resolution and mean cluster size.

The set of modules included in the May/June beamtest was largely determined by the availability of the two irradiated Outer modules, k5_305 and k5_308. Two unirradiated Outer modules, k5_310 and k5_312 were therefore also included for direct comparison. One inner (k5_304) and middle (k5_301) module were also included, as were two previously measured barrel modules as reference samples. The two irradiated modules were again studied in the July beam period.

The first goal of the beamtest program was the measurement of these important module parameters for a minimum ionising particles at normal incidence to the silicon planes. This configuration is the reference configuration for comparison with other beamtests and for parametrising the basic module performance. The detectors were biased at the nominal operating voltages, measured at the high voltage supplies, of 150 V for the unirradiated modules and 350 V for the irradiated modules representing the extremes of radiation history. Due to the voltage drop in the hybrid bias resistor the voltage on the detectors of the irradiated modules was up to 30 V lower than the output of the power supplies. Therefore, some important results will be reported for a power supply output of 400 V, corresponding to approximately 370 V on the detectors.

A second goal was the measurement of the bias voltage dependence of the modules, especially the irradiated modules, since this is important operational information. This measurement consists of repeated threshold scans at several bias voltages from which the shape of the charge collection, noise, and signal-to-noise versus bias curves can be determined.

A third goal was a mapping of the position dependence of the module performance. This was performed at normal incidence by taking threshold scans at several positions around the silicon sensitive area. This included positions near and far from the end-tap electronics hybrid position, to study effects of the distance from the readout amplifiers as well as of the varying strip pitch, as well as several positions across the module to look at the chip-to-chip variation .

In addition, measurements at angles away from normal incidence were attempted with the Atlas testbeam magnet switched on (at 1.56T nominal) and off. This study was not completed, but initial measurements confirmed expectations from previous barrel measurements.

6.4 Results.

6.4.1 Efficiency and noise occupancy.

In the test beam, the tracking efficiency is measured by requiring a hit in the binary module closer than 150 μm from the position of the track as extrapolated from the analog telescope. Efficiency versus threshold curves or S-curves are reconstructed by scanning the discriminator over a large range of values, corresponding to charges of 0.7 to 6 fC. The noise occupancy is counted in dedicated noise events taken with a software trigger in the out-of-spill periods.

Figure 23 shows the efficiency versus threshold curves averaged over both links of all non-irradiated modules, and Figure 24 the s-curves averaged over the four links of the irradiated modules. The error bars represent the standard deviation of the efficiency measurement over the full statistics.

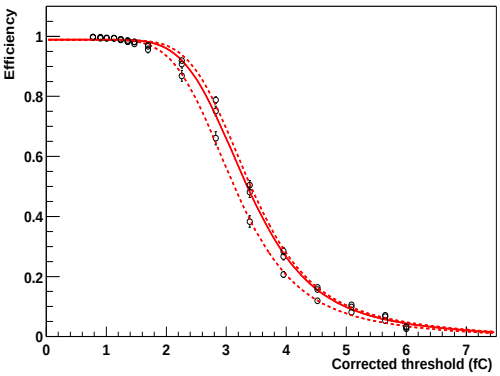


Figure 23.Efficiency vs threshold averaged over all non-irrradiated modules. The solid line represents data taken with a detector bias voltage on the power supply of 150 V, the lower and higher s-curves are from 100 and 250 V, respectively.

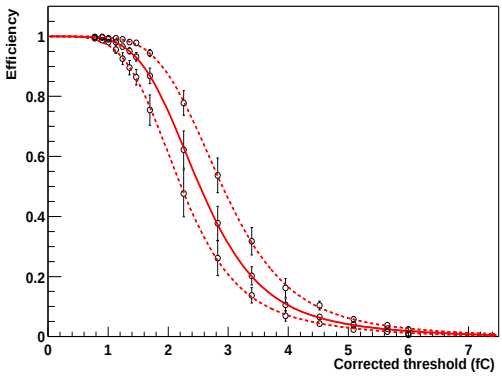


Figure 24. Efficiency vs threshold averaged over both irrradiated modules. The solid line represents data taken with a detector bias voltage on the powe supply of 350 V, the lower and higher s-curves are from 300 V and 450 V respectively.

SCT tracking specifications require high, 99%, tracking efficiency and a noise occupancy below 5×10^{-4}. Figures 25,26 and 27 provide a closer view of the efficiency around the envisaged operational threshold of 1 fC. The noise occupancy is presented on a logarithmic scale in the same figures. The specifications for the efficiency and noise occupancy are indicated as straight lines.

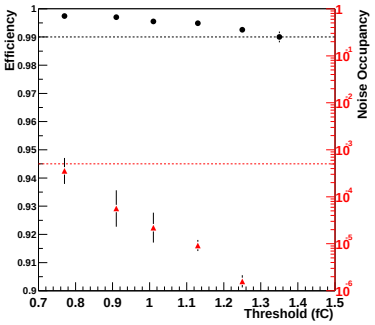


Figure 25. Closer view of the efficiency vs threshold at nominal bias voltage. Averaged over all non-irrradiated K5 modules. The noise occupancy at these thresholds is plotted in the same figure.

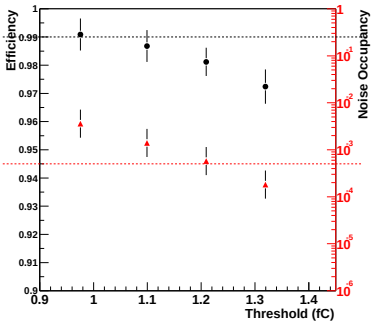


Figure 26. Closer view of the efficiency vs threshold at a bias voltage of 400 V (370 V on the detectors). Averaged over both irrradiated K5 modules. The noise occupancy at these thresholds is plotted in the same figure.

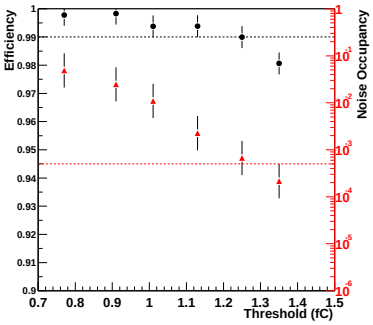


Figure 27. Closer view of the efficiency vs threshold at 450 V (420 V on the detectors) . Averaged over both irrradiated K5 modules. The noise occupancy at these thresholds is plotted in the same figure.

Table 6 lists the modules tested with a summary of the results for the most important operating parameters. The last two columns show the threshold at which the efficiency is 99% and the threshold at which the envisaged occupancy is reached, respectively. The noise occupancy at the nominal threshold meets the specified 5×10^{-4} with quite some margin for all non-irradiated modules. The noise on the inner module is significantly lower due to the lower capacitive load of the single detector on the amplifier. The noise occupancy dependence on threshold is compatible with a gaussian noise.

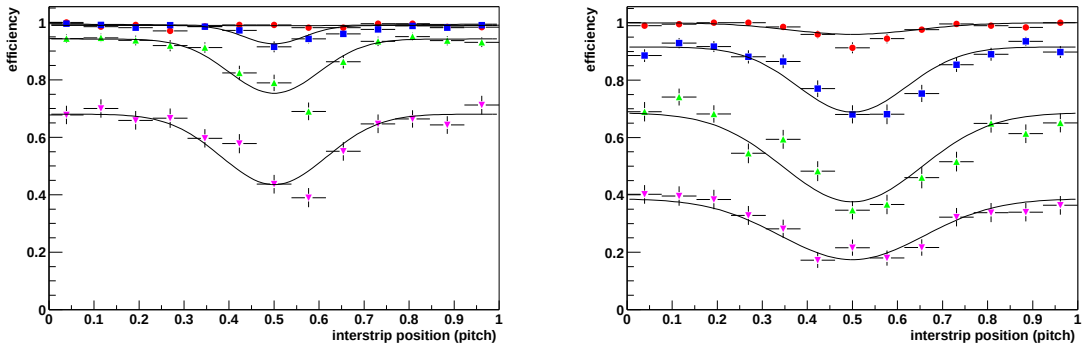
The shadowed rows correspond to the irradiated modules. Both of them, especially K5-305, show an excess of noise that is consistent with the noise levels measured in the laboratory. There is, however, for K5-308 a threshold window between 1.2 and 1.3 fC in which the efficiency and noise occupancy specifications are met. The deterioration of the signal at this bias voltage results in a signal over noise ratio of between 7 and 8, with a larger spread in the median charges. The signal over noise ration is expected to be somewhat higher in the case of middle and, especially, inner modules.

In the binary readout scheme the region right in between two strips is the weakest point in terms of efficiency, as charge sharing reduces the effective deposited charge on each strip. Figure 28 shows the dependence of the efficiency on the position of the track with respect to the two strips. For threshold higher than the nominal,

module	Eff @ 1 fC	NO @ 1 fC	Qmed (fC)	S/N	Thr Eff	Thr NO
K5-304	99.6	3×10^{-8}	3.3	20.6	<1.24	>0.78
K5-301	99.7	7×10^{-5}	3.3	13.8	<1.20	>0.87
K5-302	99.7	7×10^{-5}	3.3	13.2	<1.72	>0.92
K5-310	99.5	9×10^{-5}	3.4	14.4	<1.69	>0.90
K5-312	99.7	5×10^{-5}	3.5	13.8	<1.69	>0.90
K5-305	98.7	7×10^{-3}	2.8	7	<1.03	>1.38
K5-308	99.5	2×10^{-3}	2.8	7.7	<1.31	>1.20

Table 6. Benchmark results for the modules tested in the May 2002 beam test. The response to perpendicularly inciding MIPs is measured at nominal bias voltage. Note that the actual voltage on the detectors of the irradiated modules is around 325 Volts. Shadowed rows correspond to irradiated modules. The last two columns show the threshold at which the required efficiency and noise occupancy are reached.

charge sharing leads to a dip in efficiency in the center. In the non-irradiated modules no significant structure is seen at 1 fC threshold. In the irradiated modules, that have less charge margin, the efficiency deteriorates slightly in the central region between the two strips.



(a) outer (b) outer irradiated

Figure 28. Efficiency versus inter-strip position (in units of the pitch) for a non-irradiated and an irradiated outer module. The round markers correspond to a threshold of 1 fC. The remaining lines correspond to 1.6, 2.2 and 2.7 fC.Incidence of the beam particles is perpendicular.

6.4.2 Charge collection.

The median charge is computed as the 50% efficiency point of the s-curves. The signal-to-noise ratio is obtained by dividing the median charge by the equivalent noise charge (@ 2 fC) obtained in the in-situ calibration. Note that the noise was measured at the nominal detector bias voltage. A possible dependence of the noise with bias voltage would not be taken into account in the S/N measurement. Table 6 lists the median charge and the signal over noise for the different modules.

Calibration variations from one chip to the next can be estimated from repeated measurements with various beam positions on the modules. To this end, the chips are analysed separately and the median charge is reconstructed on each of them. The spread in the observed charges on the non-irradiated modules is around 0.1 fC (or 4 %, standard deviation) for chips on the same module, consistent with the measured spread in the calibration capacitors which is thought to be the dominant contribution to the calibration uncertainty. Within errors, the signal coincides on the three types of modules and with the signal found on a barrel module [13].

On the irradiated modules the observed spread in the median charges from different chips is quite larger: 0.2 to 0.3 fC, nearly 8%. This is true even for chips from the same wafer. The signal to noise ratio is generally much more uniform.

The detector bias voltage is an essential parameter in the operation of the module, especially so after irradiation. During the test beam, the performance of the modules was measured in a range of bias voltages. Figure 29

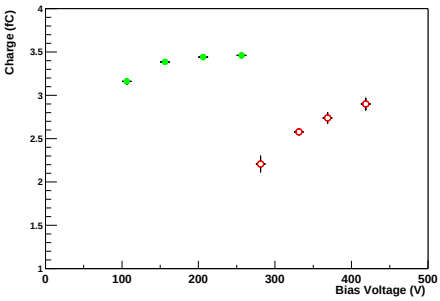


Figure 29. Median collected charge versus corrected detector bias voltage for both irradiated (open markers) and un-irradiated modules (filled markers).

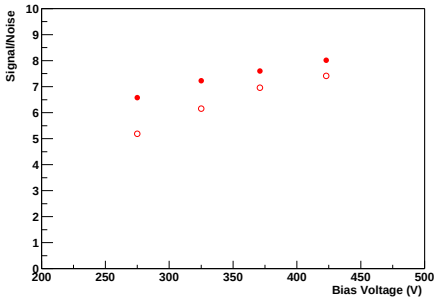


Figure 30. Signal to noise ration versus corrected detector bias voltage for both irradiated modules. Open markers correspond to K5-305 while filled ones to K5-308.

shows the median collected charge as a function of the corrected bias voltage (the voltage drop across the bias resistor on the hybrid is subtracted from the nominal value set on the HV power supply). Non-irradiated modules collect a nearly constant charge from around 120 Volts. Below that, ballistic deficit of the shaper leads to a moderate charge loss.

In the irradiated modules the voltage drop over the 11kΩ of the bias filter circuit can not be neglected. Also, much higher bias voltages are necessary to retrieve a similar signal. At the nominal detector bias voltage of 350 V around 85 % of the signal of the non-irradiated modules is collected by the irradiated modules. The signal-to-noise of the two modules is very similar at the highest bias voltage (450 V), see Figure 30 , but starts to diverge at lower voltages. This seems to indicate a different depletion voltage in both modules.

In the SCT most of the charge is collected on a single strip. Signal clusters comprising more than one strip make up a small fraction of the total and are concentrated in a narrow region in the center between two strips. The amount of charge sharing between neighboring strips is measured most sensitively as the average cluster size of signal clusters. Particles that traverse the detector at an angle have a longer path length through the silicon, leading to a larger energy deposition. When the projection of the path on the surface of the detector has a component perpendicular to the strips, charge sharing (and thus the probability of creating of two-strip clusters) increases. The cluster size in Table 7 shows the expected dependence on module type (pitch) and incidence angle.

6.4.3 Spatial resolution.

In the test beam, the spatial resolution is determined by measuring the width of the residuals - the difference between the track position (extrapolated from the telescope measurements) and the center of the binary cluster. For 1-strip clusters the spatial resolution is expected to be given by pitch/√12. The presence of multiple-strip clusters leads to a slight improvement of the resolution. The results for charge and resolution for perpendicular incidence and 8 degrees are listed in Table 7.

Module type	*Average pitch in the beam region (μm)*	*Perpendicular incidence*			*8 degrees incidence*		
		Clusize @ 1fC	*Resolution (μm)*	*Qmed (fC)*	*Clusize @ 1fC*	*Resolution (μm)*	*Qmed (fC)*
inner	~65	1.14± 0.01	18.3±0.3	3.3± 0.1	-	-	-
middle	~78	1.09 ± 0.01	22.6±0.3	3.3± 0.1	1.21± 0.01	20.6±0.2	3.2±0.1
outer	~82	1.072± 0.004	23.7±0.1	3.4± 0.1	1.18± 0.02	22.0±0.2	3.3±0.1
outer irradiated	~82	1.14± 0.04	24.4±0.3	2.6± 0.2	1.19± 0.03	23.9±0.2	2.3±0.1

Table 7. Angle dependence of a number of observables related to the spatial resolution. The average size of signal clusters (within 150 μm of the track) is a good indication of charge sharing. The resolution is relatively unaffected. . The inner module did not participate in the rotation. The beam is in the furthest wafer for both outer and middle modules.

6.4.4 Timing performance.

The timing performance of the module can be evaluated by reconstructing the response of the module as a function of time. The reconstructed pulse shapes yield an effective rise time that depends both on the electric field strength on the sensor (and, hence, the detector bias voltage) and on the intrinsic speed of the front end.

Figure 31 shows the pulse shape reconstructed in a non-irradiated module at different bias voltages and Figure 32 shows the pulse shape in an irradiated module. The irradiated modules show a clearly longer pulse, see Table 8 , due to a combination of changed detector pulse (type inversion) and a deteriorated performance of the front-end.

Module type	***outer***	***inner***	***Irradiated outer***
peaking time (ns)	23.2 ± 0.8	22.7 ± 0.4	29.2 ± 0.6

Table 8. Effective peaking time at an HV supply voltage of 150 Vols for non-irradiated modules and 350 V for irradiated modules (note that the detector voltage is around 320 V).

The increased values for the peaking time are in qualitative agreement with the increased time walk measured with the chip's internal calibration circuit.

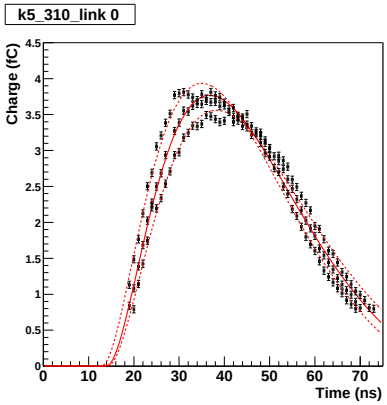


Figure 31. Pulse shapes reconstructed from a non-irradiated module. The solid line corresponds to the nominal bias voltage of 150 V. Dashed curves correspond to 100 and 250 V.

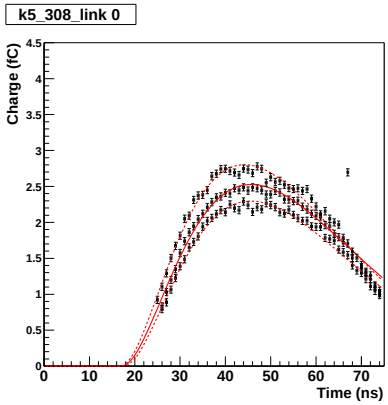


Figure 32. Pulse shapes from an irradiated modules. The solid line corresponds to a bias voltage of 350 V. Dashed curves correspond to 300 and 450 V.

6.4.5 Preliminary results from the July beam test.

Some measurements of the May beam test were repeated and extended in the July beam period. On the basis of laboratory measurements done in between both beam periods a new set of optimal front-end settings was chosen. Moreover, the analog supply voltage was raised to Vcc=3.8 V. Improvements in the way the module was cooled allowed for a hybrid temperature of -2 degrees and for the bias voltage to be raised up to 600 V, since the module was thermally stable. Preliminary results from these tests on the K5_308 are reported in this section.

module	***Eff @ 1 fC***	***NO @ 1 fC***	***Qmed (fC)***	***S/N***	***Thr Eff***	***Thr NO***
K5_308	99.4	4×10^{-3}	2.7	7.5	<1.20	>1.20

Table 9. Preliminary benchmark results for the K5_308 module tested in the July 2002 beam test. The response to perpendicularly inciding MIPs is measured at a bias voltage of 400 Volts at the power supply. Note that the actual voltage on the detectors is around 370 Volts. The last two columns show the threshold at which the required efficiency and noise occupancy are reached.

Figures 33 and 34 show the tracking performance, efficiency and noise occupancy, of module K5_308 as measured with perpendicular incident tracks in the July period. Table 9 summarizes the benchmark performance parameters. Given the changes in the way the module was operated the agreement with the May results is rather good.

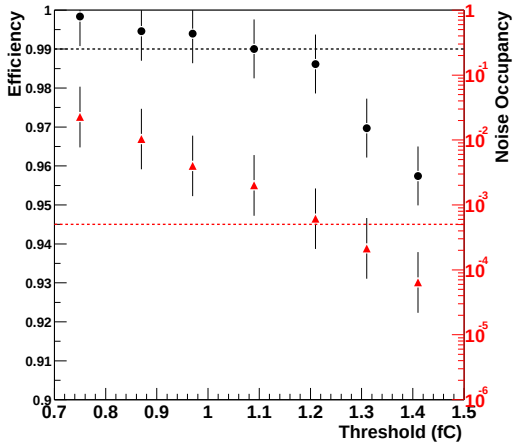


Figure 33. Closer view of the efficiency vs threshold of K5_308 at a bias voltage of 400 V (370 V on the detectors). The noise occupancy at these thresholds is plotted in the same figure.

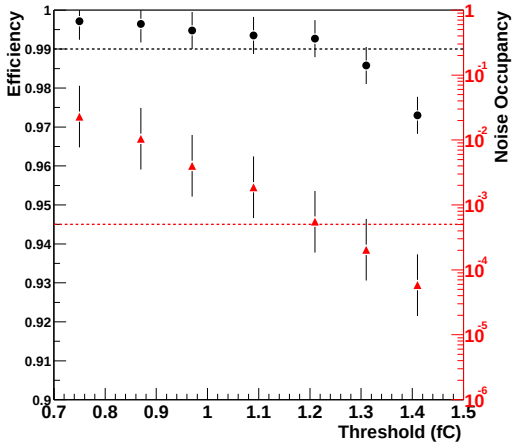


Figure 34. Closer view of the efficiency vs threshold of K5_308 at a bias voltage of 500 V (470 V on the detectors). The noise occupancy at these thresholds is plotted in the same figure.

The improved cooling allowed to go up to higher voltages and study the charge collection up to 600 V. The charge and signal to noise ratio of K5_308 are compared to the response of non-irradiated modules in figures 35and 36.

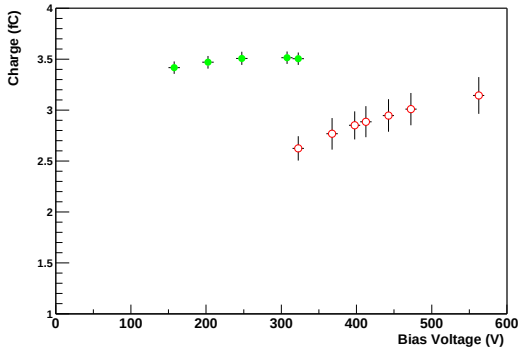


Figure 35. Median collected charge versus corrected detector bias voltage for both irradiated (open markers) and un-irradiated modules (filled markers).

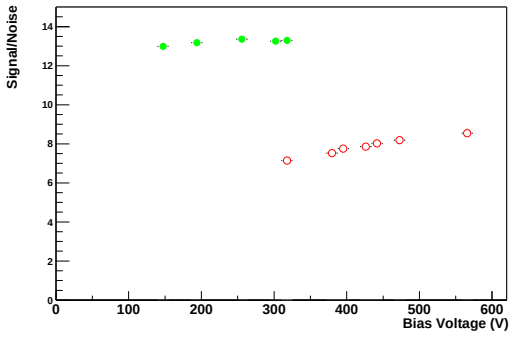


Figure 36. Signal to noise ratio versus corrected detector bias voltage for both irradiated (open markers) and un-irradiated modules (filled markers).

During the July and May beam test data were taken routinely with the beam inciding on the wafer closest to the hybrid (W31). In July, a number of threshold scans at different bias voltages were repeated after changing the position of the beam to the further wafer (W32). As the beam still falls on the region read out by the same chips, this measurement does not suffer from the uncertainty in the calibration present when comparing results from different chips. The influence of the pitch on the collected charge is expected to be small. Therefore, these scans give an idea of the variation of the collected charge between detector wafers. From the two pairs of wafers on K5_308 one yields results that agree to within 0.1 fC. The other pair, however, a charge is found in W32 wafer that is 0.3 fC higher than in the W31 wafer.

The shaper pulse reconstructed from the test beam data is now significantly faster than when it was measured in the May test beam. The pulse shapes in Figure 37 correspond to supply voltages of 350, 400 and 500 V. The effective peaking time at a bias voltage of 350 V is approximately 26 nanoseconds.

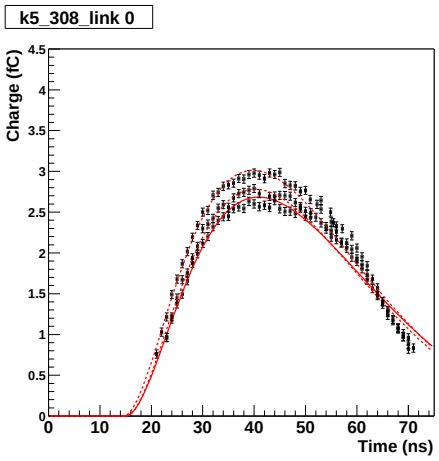


Figure 37. Pulse shapes for an irradiated module. The solid line corresponds to a supply voltage of 350 V. Dashed curves correspond to 400 and 500 V.

7 Summary.

The SCT end-cap modules satisfy the electrical performance goals described in [3], with the exception of a slightly higher final post-irradiation noise value. However, noise occupancy and efficiency specifications are met for three out of 4 modules selecting a slightly higher than 1 fC operating threshold, which has no consequence on the final tracking efficiency and reconstruction. The modules can be operated in a stable fashion at more than the nominal 500 V detector bias voltage. The first results from the system test are encouraging.

8 References

[1] ABCD3T specifications.

[2] W. Dabrowski et al. *Progress in Development of the Readout Chip for the ATLAS Semiconductor Tracker*. Proceedings of the Sixth Workshop on Electronics for the LHC Experiments (LEB2000), Krakow, September 2002.

[3] Electrical Specifications and Expected Performance of the End-cap Module, ATL-IS-EN-0008.

[4] http://sct.home.cern.ch/sct/sctdaq.html

[5] http://atlas-sct-irradiation.web.cern.ch/atlas-sct-irradiation/default.htm

[6] A. Greenall, C. Macwaters and T. Weidberg. BER testing of optolinks wit K5. http://www-pnp.physics.ox.ac.uk/~weidberg/K5_BERscans.doc

[7] SCT End-cap System Test Sector Prototype. ATL-IS-AN-0005.

[8] N. Spencer. *ATLAS SCT / Pixel Grounding and Shielding Note.* *http://scipp.ucsc.edu/groups/atlas/elect-doc/SCT_GND_SHIELD2.pdf*

[9] Grounding and Shielding for the SCT End-cap. ATL-IS-ER-0019.

[10] *ATLAS SCT - End-cap Grounding and Shielding. ATL-IS-EN-XXXX*

[11] http://alpha.ific.uv.es/sct/activities/electronics/VAL_K3-165_temp/ http://alpha.ific.uv.es/sct/activities/electronics/VAL_K3-166_temp/

[12] Barrel Module FDR. Electrical Test performance document.

[13] SCT H8 Atlas note. ATLAS-INDET-2002-005.