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Design optimization of silicon microstrip detector modules for operation in high radiation levels at the LHC.

C. Lacasta[a1]

[a]*Instituto de Física Corpuscular (IFIC) - CSIC/Univ. de València*

representing the ATLAS SCT collaboration

Abstract

The Large Hadron Collider (LHC) operation conditions amount to considerable challenges in track and vertex detector design, which is driven by many conflicting requirements. The high luminosity, 10^{34} $cm^{-2}s^{-1}$, planned for the 10 years of LHC operation are at the expenses of a very high particle interaction rate, ~10^9 Hz and, hence, high radiation fluences, about 2×10^{14} n_{eq}/cm^2 total hadron fluence. Such a luminosity is achieved using a bunch-bunch crossing frequency of 40 MHz that will require very fast and low noise signal processing, in order to separate signals from different bunch crossings, very long on-detector buffers to keep the data during the trigger latency together with fast and reliable data links for the off-detector data transmission. Since radiation effects are strongly temperature dependent, the thermal properties of the devices will drive severely the design options. This, together with the stringent requirements set by the expected performance of the LHC trackers translates into constraints on the mechanical precision and stability. Last but not least, access for maintenance and repair will be very restricted and, since radiation damage is severe, redundancy is another key point in the design. This paper describes the design options chosen for the ATLAS Semiconductor Tracker (SCT) modules and will show results on their performance.

Keywords: silicon, microstrip, detector, module, ATLAS, SCT

1 Introduction.

ATLAS [1] is a general purpose detector designed to exploit the full discovery potential of the Large Hadron Collider (LHC). The Inner Detector [2] (ID) , enclosed in a 2 T solenoid field, provides with track finding, momentum and vertex measurements together with enhanced electron identification. This is achieved by a combination of discrete high resolution pixel and strip detectors as well as continuous straw-tube detectors with transition radiation capability.

The ATLAS Semiconductor Tracker (SCT) is the silicon microstrip tracker of the ID. It covers from 30 to 56 cm in radius from the beam axis, and 541 cm along the beam axis. The layout of the SCT will consist of 4 central layers (barrel) and 9 disks in each of the forward and backward directions, as shown in

[1] Corresponding author. Tel.: +34 96 398 3490; fax: +34 96 398 3488; e-mail: Carlos.Lacasta@ific.uv.es

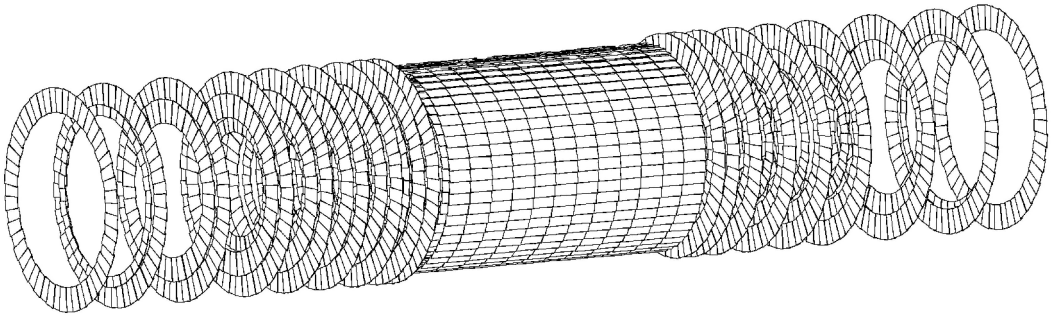

Figure 1. SCT layout showing only the silicon sensors.

Figure 1, providing a minimum of 4 points per track and an active silicon area of ~63 m^2. It will be placed between the silicon pixel detector and the transition radiation detector of the ID.

2 Motivation of the design.

The SCT will be composed of about 4000 detector modules with a total of about 6.3×10^6 readout channels. The basic readout unit o the SCT is the so called module. It consists of a set of single sided, ac-coupled, *p in n* silicon microstrip detectors glued back to back, with the strips forming a stereo angle of 40 mrad to provide two coordinates. An electronics package for the binary readout of the sensors, and an interface to the cooling and mechanical support structure of the tracker are also part of the module.

An efficient and accurate track and vertex reconstruction imposes to the SCT a detector efficiency of 95% over the lifetime of the experiment, an Rϕ accuracy of 17 μm at the SCT radius, a resolution of 580 μm for the second coordinate -R, for the forward modules, and z in the barrel-, and a minimum radiation length. This is to be achieved by a detector concept that has to be hermetic to tracks with p_T>1 GeV/c. Furthermore, tracking will be used to provide a second level trigger threshold on transverse momentum and, therefore, absolute ϕ positions of any strip need to be calculated without using stereo information.

As a consequence, a very precise location of the modules on the support structure and module assembly is required: ~5 μm across the strips positioning the wafer in the back-to-back pair, ~25 μm along the strips and ~50 μm in module thickness. Thermal and mechanical constraints conflict with the fact that the material budget of the SCT has to be minimum. The materials used in the module should, therefore, be low mass but still with good thermal and mechanical properties.

The operation of the modules in the LHC environment poses a number of conflicting requirements on their design. The high luminosity, 10^{34} $cm^{-2}s^{-1}$, planned for the 10 years of LHC operation is at the expenses of a 40 MHz beam crossing frequency, very high particle interaction rate, ~10^9 Hz, and a maximum total hadron fluence of 2×10^{14} n_{eq}/cm^2. Since radiation effects are strongly temperature dependent, the thermal properties of the module drive severely the design options since the SCT will undergo temperature cycling over the range -15ºC to +25ºC and it must be safe, in the event of cooling or local power fluctuations, at temperatures up to 50ºC. This, together with the stringent requirements set by the expected performance of the tracker, translates into constraints on the mechanical precision and stability of the module whose permanent deformations should be <5 μm and the elastic deformations, occurring across the full temperature range, smaller than 50 μm.

The sensors need to be radiation resistant and, given the reduced repair and maintenance possibilities, key aspects are stable high voltage operation and efficient charge collection. The severity and consequences of the high accumulated radiation levels for silicon detector operation,

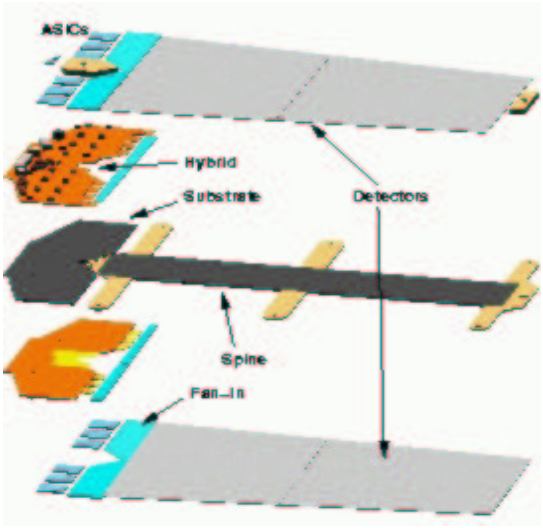

Figure 2. Exploded view of an end-cap module.

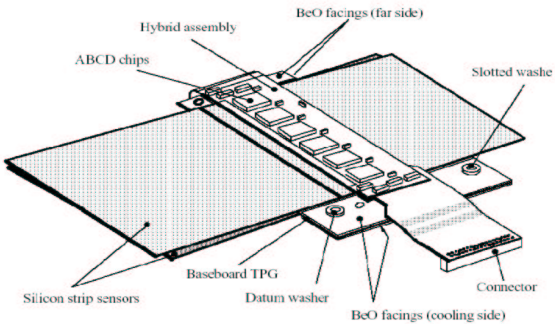

Figure 3. Barrel module.

causing increased leakage current and type inversion, give rise to the need to operate the detectors at -7ºC. The corresponding depletion voltage will be in the range 300-400 V, depending upon warm-up scenarios. This will result in a total leakage current of about 800 nA. Thermal considerations and, specially, concerns of thermal run-away, lead to a module design where the effective in-plane thermal conductivity must be increased beyond that of silicon. This is achieved by the use of thermal heat spreading materials that are laminated as part of the detector sandwich.

The readout electronics should be radiation resistant, up to 10 Mrad, high speed, ~20 ns peaking time, with low noise to keep the occupancy at reasonable levels, very long on-detector buffers, about 2.5 μs, to keep the data during the first level trigger latency time and low power consumption, 5.5W nominal and 7.2 W maximum for a whole module. Since radiation damage is severe, redundancy is another key point in the design. The Atlas Binary Chip DMILL (ABCD [9]) has been design to meet the imposed requirements. It has been fabricated using the Radiation Hard DMILL technology [8] and implements a binary readout architecture. Binary readout presents the advantage of a higher data transmission bandwidth, requirements on the quality of data links are less stringent, and requires a simpler off-detector electronics. On the other hand, it is less immune to external electromagnetic interference (common-mode) and special care has been taken in the design and grounding of the system to avoid that problem.

The data transmission off detector is also an important issue given the huge data rates expected: 35 Mb/s per module with less than 0.1% data losses. A system based on optical fibers has been designed to meet these requirements because of its low mass and lack of electrical pickup.

3 Module design.

There is a single module design for the SCT barrel region, and three designs for the various radial locations in the SCT forward regions. The module design follows, however, the same concept. Figure 2 shows an exploded view of an end-cap outer module and Figure 3 shows a barrel module.

The module has two differentiated parts, the hybrid, a Cu/Polyimide flexible circuit laminated onto a carbon-carbon substrate , which is the support of the readout ASICs, and the detector section. Both are thermally decoupled. The barrel module has two single sided hybrids bridged over the detector and the cooling contact is made at one side, as shown in Figure 3. The end-cap module has one double-sided hybrid set at one end of the module. The detector section and the hybrid are separated by a thermal break bridged by fan-in structures used to connect the strips to the ASICs. The primary cooling contact is at this break, along the module axis. Additional cooling is provided by a contact to the far end of the detector section.

In the detector section, silicon sensors are glued either side of a spine or baseboard which acts both as a mechanical spacer and a high thermal conductivity heat spreader, providing the module with the appropriate mechanical rigidity. In all but one of the designs two detectors are daisy-chained on each side, giving an active strip length of about 12 cm, which is constrained by the capacitive load of the readout ASICs and by the occupancy at high luminosities. The strips on opposite sides are rotated by a stereoangle of 40 mrad, that will provide z/R measurement capability. The choice of a small stereoangle has been dictated by a compromise between the resolution on z/R, and therefore on vertex/mass reconstruction, and the need to reduce the number of ghost hits near a real track in high multiplicity events.

A binary architecture has been chosen for the readout of the sensors which dictates the readout of individual strips, rather than charge division. The required tracking precision in Rϕ is, therefore, obtained by an 80 μm pitch, giving an intrinsic point resolution of 23 μm and a space point resolution of about 19 μm. While the pitch is constant in the barrel modules, for the forward modules the strips run approximately radially outwards from the beam axis. In the barrel region the modules are mounted at an angle of 10° to the tangent so as to minimise the signal spread during operation in the solenoidal field.

The ASICs dissipate a power of 6 W for nominal operation, and a maximum of up to 8.1 W. As the dose accumulates, the heat generation in the sensor bulk becomes appreciable due to the increase of leakage current which, in his turn, roughly doubles every 7°C being, therefore, a potential source of uncontrolled temperature rise: the so called thermal runaway. To avoid thermal runaway the effective in-plane thermal conductivity must be increased beyond that of silicon, and this is achieved by the use of adequate materials for the spine or baseboard onto which the sensors are glued. The material chosen has been a pyrolytic graphite (TPG or VHCPG) with an effective in-plane thermal conductivity of 1500-1700 W/mK at 20°C, which increases by 0.4% for each degree of temperature decrease, and a transverse thermal conductivity of typically 8 W/mK.

Table 1.
Sensor Geometries. All sensors are 285 μm thick. Dimensions are in mm, strip pitch in μm and interstrip angle in μrad.

	Barrel	W12	W21	W22	W31	W32
Length	64.000	61.060	61.085	54.435	65.540	57.515
Outer width	63.360	55.488	66.130	74.847	64.636	71.810
Inner Width	63.630	45.735	55.734	66.152	56.475	64.653
Strip pitch	80	57-69	70-83	83-94	71-81	81-90
Interstrip angle	0	207	207	207	161.5	161.5

Table 2.
Substrate and design differences between manufacturers

	Hamamatsu	CiS
Sensor shapes	All	Wedges only
Orientation	<111>	<111>
Oxygenation	None	W12 only
Biasing resistor	Polysilicon	Implant
Edge design	Single guard	14-multiguard
Strip dielectric	Composite structure depending on manufact.	

4 Module components.

4.1 Silicon microstrip detectors.

Silicon microstrip *p in n* detectors, with 768 ac-coupled readout strips have been chosen as the technology for the SCT. The strips are biased through a polyisilicon or implant resistors from a common bias line which surrounds all strips on a wafer. The detector edge and guard ring design varies depending on the manufacturer. The sensors are supplied by Hamamatsu [3] and CiS [4]. They have two basic shapes. The barrel region uses rectangular shaped sensors with parallel strips, and the end-caps wedge shaped sensors with radial strips. Due to varying coverage requirements in the forward wheels, there are five minor variations in the size of the wedge sensors. The geometries are summarised in Table 1, while the main design and processing differences between manufacturers are outlined in Table 2.

Sensors accepted for use in the construction of the SCT have been subjected to an extensive qualification program [5]. Table 3 lists the main

Table 3.
Main specifications of the sensors after being irradiated with 3×10^{14} p/cm^2.

V_{dep}	350 V for > 90% CCE
$C_{interstrip}$	<1.5 pF/cm @ 350 V, 100kHz
R_{BIAS}	~1.25 MΩ
$I_{leakage}$	<250 μA up to 450 V (-18ºC)
Microdischarge	< 5% increas in noise for 300-400V
Good strips	>99% at 350V

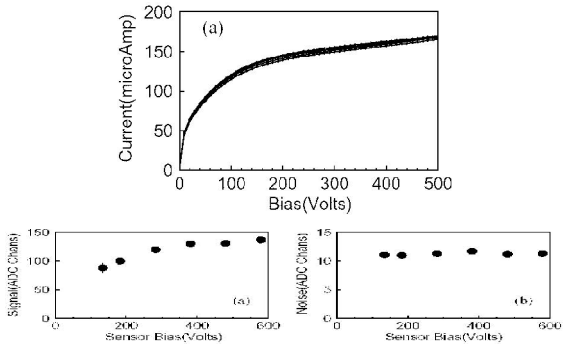

Figure 4. Typical post-irradiation characteristics of the sensors. Top figure shows the IV curve for various sensors at -18ºC and the bottom the signal and noise, as measured with fast analogue electronics, versus the bias.

specifications of the sensors after irradiation to 3×10^{14} p/cm^2. Figure 4 shows some typical measurements made on irradiated detectors showing a leakage current of about 150 μA at 500 V and a signal over noise ratio above 10.

The extreme levels of radiation during the experiment will cause increased leakage currents and type inversion to take place within the silicon bulk early on in the experiment lifetime, making the detector junction to move to the back side of the sensor after inversion. High depletion voltages will, therefore, be needed to ensure the full depletion so that charge is efficiently collected. Figure 4 shows that the collected charge reaches the plateau at about 350 V. The system will, thus, be required to operate reliably up to 500 V. Irradiated detectors will, in addition, anneal at temperatures above 0ºC [6,7]. Although in a short time scale the annealing will reduce the depletion voltage with time, at much longer time scales it will start increasing. Leakage current can be reduced and annealing effects can be suppressed by operating the detectors below 0ºC. It is for this reason that the SCT will be maintained at -7ºC whilst in operation.

4.2 Readout ASICs.

The ABCD3T chip is a single chip implementation of the binary readout architecture for silicon strip detectors in the SCT. It comprises front-end circuitry, employing a bipolar transistor in the input stage, discriminators, binary pipeline, derandomizing buffer, data compression logic and the readout control logic. There are 128 readout channels on a 6.6×8.4 mm^2 die which contains about 30000 bipolar and 200000 CMOS devices. The chip is manufactured in the DMILL radiation-hardened BiCMOS process.

The key requirements for the front-end are low noise, low power and efficient identification of the beam crossings. The 25 ns peaking time is short enough to keep the time-walk in the range of 16 ns and the double peak resolution below 50 ns, ensuring that the fraction of events shifted to the wrong beam crossing is below 1% and that less than 1% of the data will be lost at the highest occupancies. Noise has been optimised for the relative contributions of series and parallel noise sources given a total strip capacitance in the range 15-20 pF. To compensate the expected β drop after irradiation, a 5-bit DAC has been implemented in the chip to adjust the collector current of the input stage and optimise the noise performance. In addition, the bias current in the following stages is also controlled by another 5-bit DAC which allows to adjust the DC biasing of the circuit and compensate for the decrease of β. Considering the irreducible noise sources, a signal over noise factor of 15 is expected at the beginning of the experiment, and 10 after the irradiation of the sensors and the electronics.

The preamplifier-shaper stage is followed by a discriminator with a common threshold for all the 128 channels that is controlled by an 8 bit DAC. The SCT aims to operate with a threshold of 1 fC in order to be efficient for the inclined tracks. To maintain the channel-to-channel variation of the threshold below

4%, specially after irradiation, the ABCD3T implements an individual threshold correction in each channel with a 4 bit DAC, with four selectable ranges.

Data from the discriminator output is latched in the input register, either in edge sensing or level mode, every 25 ns and clocked into a 132-cell pipeline, that matches the first level trigger latency time. Upon reception of a trigger signal, the data are transferred from the pipeline to the second level buffer, eight events deep. Data is them compressed by the data compression logic and readout via a token ring, allowing for the readout of six chips through a single optical link.

The electronics operates at at average trigger rate of 100 kHz with a minimum spacing between consecutive triggers of 2 bunch crossings; statistical variations in trigger arrival beyond this must introduce less that 1% data losses for 1% occupancy. This drives the bandwidth of data links and the depth of the derandomising buffer.

The chip uses two power supply voltages: 4 V for the digital part and 3.5 V for the analogue one. The total power consumption is 3.2 mW/channel for typical operating conditions.

On top of that, the ABCD3T implements a calibration circuitry and a redundancy mechanism that redirects the output and the readout control signals of the chip so that a failing die can be bypassed.

Extensive studies made on the ASICs [10,11] with the 24 GeV proton beam and X-ray facility at CERN, 200 MeV pion beam at PSI, neutrons from the TRIGA reactor in Ljubljana and the ^{60}Co source at Santa Cruz, California, USA, show that the ABCD3T and the DMILL technology, in which the chip has been realised, meet the requirements with respect to radiation hardness.

4.3 Off-detector data transmission.

Because of its low mass and lack of electrical pickup, optical links will be used in the SCT to transmit data from detector modules to the off-detector electronics at a rate of 40 Mbits/s per link. Optical links will also be used to distribute timing, trigger and control (TTC) data from the counting room to the front-end electronics. The components in the system are illustrated schematically in Figure 5.

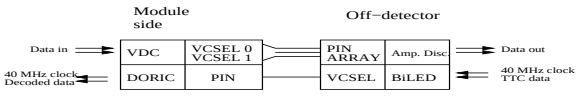

Figure 5. ATLAS SCT optical link components.

Data will be transmitted off the module by two data fibres each transferring data at 40Mbits/s. The TTC data for each SCT module will be distributed by optical fibre. Bi-phase Mark encoding will be used to encode the control data on top of the 40 MHz bunch crossing clock. The links are based on radiation-hard VCSELs and PIN diodes. VCSELs are made from GaAlAs multiquantum well structures emitting at around 850 nm and the optical receivers are epitaxial silicon PIN diodes.

On the module side, see Figure 5,the VCSELs will be driven by a simple VCSEL driver chip (VDC). The PIN diode signal is received by the DORIC chip, that has a low noise preamplifier followed by circuitry for decoding the Bi-phase mark TTC data to provide the 40 MHz clock and the commands for the SCT module. The VCD and the DORIC have been design in the AMS 0.8 µm BiCMOS process. This is not usually used as a radiation tolerant process, but a sufficiently radiation tolerant design has been achieved for the use in the SCT.

The system contains immunity to single point failure. If a data link fails then the data can be routed through the other fibre of that module. If a TTC link fails, the TTC data can be taken from a neighbour module.

Extensive tests have been done [12] that prove that the system is sufficiently radiation tolerant to operate during the detector lifetime. There will be a significant SEU rate during operation at peak luminosity. SEU events may fake a genuine signal in the DORIC4, but its rate can be controlled and kept to an acceptable level increasing the amplitude of the TTC data and, correspondingly, the effective threshold.

Although the concept and components are the same both in the barrel and in the end-cap modules, the VDC and the DORIC4 chips will be mounted on

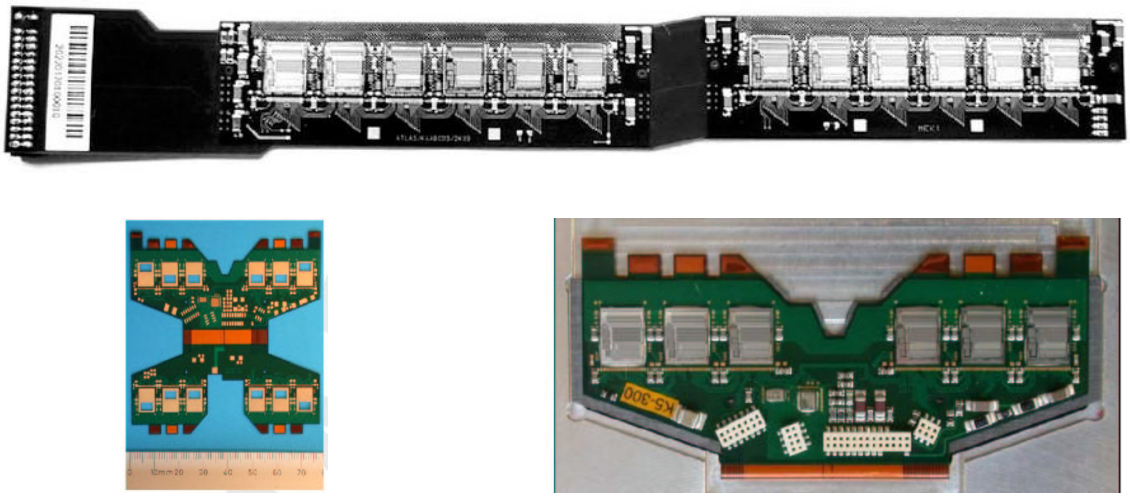

Figure 6. The top picture shows the barrel hybrid fully populated. The bottom left picture shows the forward hybrid unpopulated and the right bottom picture shows the forward hybrid fully populated and laminated onto the substrate.

the hybrid for the latter and on separated kapton tapes on the former.

4.4 Hybrids.

The readout ASICs will be mounted in a Cu/Polyimide, multilayer, flexible circuit laminated onto a carbon-carbon substrate. The same technology is used in both barrel and end-cap modules.

The hybrid plays a major role in the electrical readout as well as in the mechanical support and cooling since it is part of the mechanical linkage between the silicon sensors and the cooling systems. It must have sufficient thermal conductivity to allow most of the heat generated by the front-end chips to be removed by the coolant and must support the front-end ASICs sufficiently to allow reliable wire-bonding to the detectors. The circuitry in the hybrid distributes and filters the power. Provides ground, clock and control lines to the ASICs, supplies and filters the bias voltage to the detectors, returns the data to the optical links and supports the redundancy mechanisms of the ASICs.

For the hybrid substrate the primary concerns are radiation length and thermal conductivity. Carbon-carbon with fibers running in one direction is the preferred option. It has a thermal conductivity of about 700 W/m/K along the fibres and about 20 W/m/K perpendicular to them.

The barrel hybrid has been design as two hybrid circuits with a flexible wrap-around connection in between as illustrated in Figure 6. The main hybrid sections are built with four copper layers and they are connected by a two layers interconnect region, the wrap-around. One end is connected to the pigtail cable that has the connector at the edge. These two cable sections are the extension of the two central layers of the hybrid sections so that hybrids and cables are made in one-piece. Electrical connections among different layers are realised by either through holes, penetrating all layers, or laser-cut via-holes between two adjacent layers. Seventeen thermal through-holes are added underneath the analogue part of each ASIC. They are vertical copper holes filled with thermally as well as electrically conducting glue. This ensures thermal and electrical connections between each chip and the substrate. Hybrid temperatures can be monitored with two thermistors, one per side.

The forward hybrid, Figure 6 bottom, is a double-sided device carrying 6 readout ASICs on each side. It also incorporates the opto-chips. It is composed of six layers of copper traces in the main sections, while in the wrap-around it is reduced to two metal layers.

Electrical connection between layers is established using laser-cut micro- vias.

There is a cut-out at the center of the hybrid to locate the mounting and cooling point. In this region the analogue ground plane is continued by a copper metalization on the substrate. To reinforce the connection between the front and back sides, established through the wrap-around, voltage and ground planes are connected also by means of little finger-like extensions of the flex at the hybrid front edge. A thermal plug under each ASIC ensures a good thermal contact between the chip and the substrate. It is implemented as a window in the flex in which an AlN plug is glued so that its top surface aligns with the top surface of the flex. The plugs are staggered in order to optimise the use of the directionality of the fibres in the substrate. The temperature of the hybrid is measured by a thermistor located on top of the hybrid.

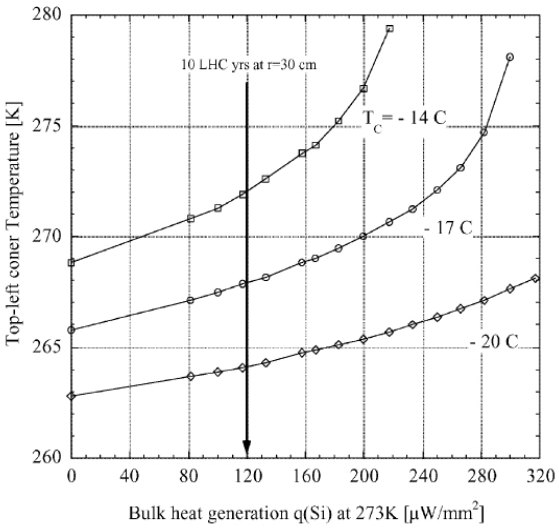

Figure 7. Temperature of the furthest corner of a sensor in a barrel module as a function of heat flux with three coolant temperatures, T_c.

5 Thermal performance of the modules

The evaporative cooling system for the SCT is foreseen to have an effective coolant temperature around -17ºC. The module design must ensure that the ASICs and the sensors are sufficiently well cooled throughout the module lifetime. As already mentioned, thermal runaway concerns, sensors' leakage current and annealing lead to operate the SCT at a temperature of -7ºC.

The bulk heat generation after 10 years of operation at LHC is estimated to be 120 μW/mm^2 in the worst case. Including a safety factor of two, the goal for thermal runaway is set at 240 μW/mm^2. Extensive FEA simulations and thermal measurements confirming the simulation have been carried out to understand the thermal performance of the modules. Figure 7 shows the temperature of the furthest sensor corner a a function of the bulk heat generation at three coolan temperatures in the case of ASICs' power at 8.1 W. The simulation shows that the thermal runaway occurs at 220 μW/mm^2 at -14ºC.

Similar analysis have been done on forward modules indicate that the thermal runaway occurs at 210 μW/mm^2 for a coolant temperature of -15ºC. A slight decrease of coolant temperature to -17ºC allows to operate the module at 240 μW/mm^2.

Simulations and measurements of the thermal profile of the modules show that the hybrid and the sensors are well decoupled thermally in both the barrel and the forward designs.

6 Electrical performance of the modules

In order to ascertain the electrical performance of the SCT modules a number of test set-ups of increasing complexity have been developed. Individual modules are first tested on the electrical stand to characterise the basic front-end parameters and demonstrate their functionality. Several modules are then mounted in a replica of a barrel or end-cap sector and operated in an environment as close as possible to the the planned ATLAS configuration in terms of cooling, power distribution, grounding and readout. This system test evaluation should demonstrate the robustness of the system as a whole and check for potential problems like crosstalk, analog-digital interference and optimal grounding. Modules are mounted on a sector of a barrel cylinder and a section of an end-cap disk. They were constructed for the system test with the emphasis set in being as close as possible to the final

configuration. Most of the components of the system, tapes, power supplies, cooling pipes and fibres, are the final prototypes of the SCT design. Also test beam measurements are made on non-irradiated and fully irradiated modules.

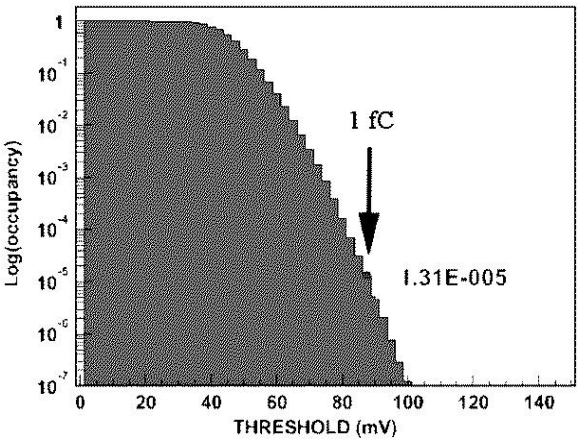

Figure 8. Mean noise occupancy of all the channels of a module meassured warm.

At room temperature the measured noise in non irradiated modules is in the region 1400-1700 e^- ENC. At the operating temperature of ~0ºC on the hybrid, the noise is reduced to typically about 1350 e^- ENC for the barrel modules and about 1450 e^- ENC for the end-cap modules with 12 cm effective strip length and 1000 e^- ENC for the 6 cm modules. The excess noise in the long end-cap modules is understood in terms of the higher strip resistance at the input of the ASICS since the hybrid has end-tap configuration. This corresponds to an expected S/N value better than 15. No difference in performance is appreciated between the electrical stand and multi module system test measurements.

The SCT aims at operating the modules with a threshold set to an equivalent input charge of 1 fC. This value is determined by minimising noise occupancy in the detector while maintaining maximum signal sensitivity also for inclined tracks that share charge between strips. Tracking as well as DAQ considerations set a limit of 5×10^{-4} for the noise occupancy in irradiated modules. On no-irradiated modules noise occupancy values of 1-2×10^{-5} have been measured at 1 fC, while for irradiated modules the value is 2-3×10^{-4}. Figure 8 shows the noise occupancy of a module measured at room temperature with non-irradiated sensors. Its smooth gaussian shape is a strong evidence of the electrical stability of the module. No differences in performance have been observed when comparing the results with the tests made on individual modules.

The performance of irradiated and non-irradiated modules has repeatedly been verified in test beams at CERN and KEK [14,15]. Modules were mounted inside a cold box between reference detectors that provided track reconstruction in 4 X-Y planes. Modules were operated at a hybrid temperature of 0ºC. The beam test provides information on charge collection, efficiency, spatial resolution, pulse shape and noise performance.

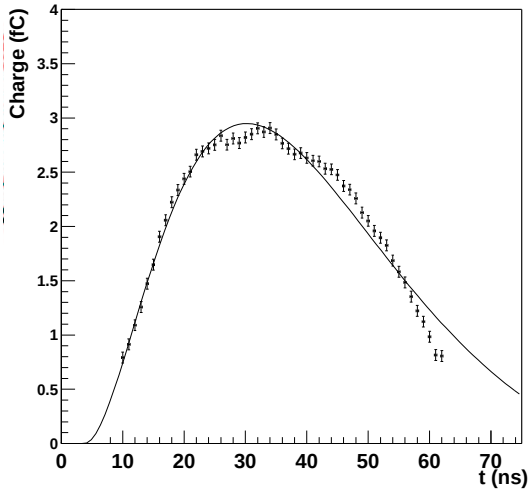

Figure 9. Pulse shape of an irradiated module.

The median charge, obtained from the 50% efficiency point in threshold scans is shown in Figure 10 for irradiated and non-irradiated modules as a function of the bias voltage. It can be seen that it saturates at about 150 V for non-irradiated and 350 V for irradiated modules.

Figure 9 shows the median charge at 350 V for an irradiated module as a function of the time delay between the trigger and the ASICs' clock edge. It provides a measure of the average shape of the pulse at the input of the discriminator. Fits to the ideal CR-

RC^3 are also shown. The peaking time of the pulse is 25 ns.

The efficiency of the irradiated modules is greater than 99% and the noise occupancy measured at 1 fC is $4x10^{-4}$ as illustrated in Figure 11.

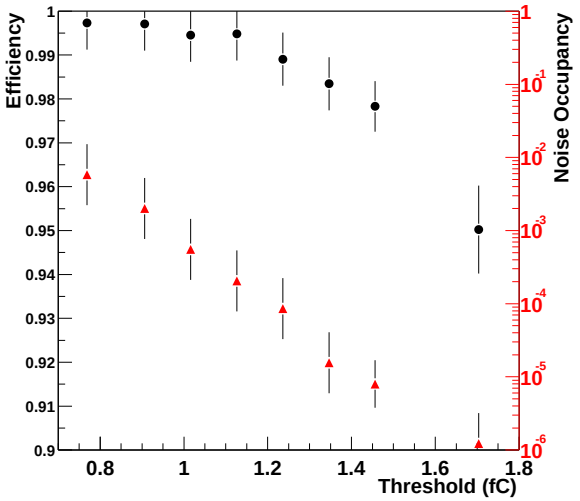

Figure 11. Efficiency and noise occupancy.

The measured spatial resolutions, 23 μm for barrel modules and 26 μm for the end-cap modules, are consistent with their respective strip pitch.

7 Summary.

The SCT module program, both on the barrel and the forward design has terminated its R&D program and it is entering into the production phase. Many new technologies have, for the first time, been successfully employed in the design and working solutions have been found to unprecedent technology challenges in the construction of silicon detector modules. The quality and robustness the the microstrip sensors have been demonstrated and the production is foreseen to be finished in short. The design of barrel modules has been carefully evaluated, found to fulfill the required specifications and it is now in full series production. As for the forward module, the final design review will take place in short and full series production will start at the beginning of 2003.

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