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TEST ON ABCD CHIPS

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Abstract

The ABCD chip is one of the two technological options for the binary readout architecture under development for the Silicon Tracker (SCT) in ATLAS. The chip is realised in the DMILL technology (a 0.8 μm BICMOS trench isolation process). This note reports on the first results obtained at CERN on the p-type ABCD chips of the first batch delivered by TEMIC in February 1998.

1 ABCD chips

The ABCD [1] design groups together the front-end and readout functions in a single chip. The main blocks of the design have been prototyped in the chip SCT128B [2]. The ABCD comprises 128 channels of the front-end circuitry (each channel built of a fast transimpedance preamplifier, a shaper of 20 ns peaking time and a discriminator), an input register, a binary pipeline, a derandomizing buffer and a sparse readout logic. In addition it includes an internal calibration circuit, internal bias generators and a DAC for the discriminator threshold control.

The chip has the possibility of latching the data either in the level sensing mode or in the edge sensing mode combined with four different data compression criteria. The analysis presented here is based on ABCD data taken enabling the edge detection circuitry in the input register. The "edge data compression criteria" (01X) has been chosen as the default readout mode.

2 Single ABCD chip on the PCB support card

Single chips were placed on a dedicated evaluation board (PCB) in order to measure in detail the analogue performance of the ABCD front–end circuitry. The goal was to extract the basic parameters of the chip in an environment as clean as possible in which an optimum working point could be found easily.

2.1 Test setup and testing procedures

The setup used to drive the chip and read back its data is sketched in Fig. 1. The basic blocks of the setup are:

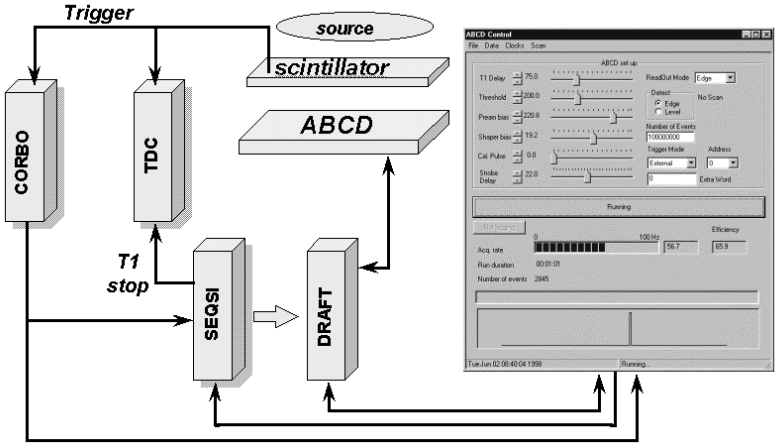


Figure 1: *Set up used for single ABCD chip tests*

- a VME crate, controlled by a National Instruments VXI controller, that housed a
- SEQSI, a programmable multi-channel sequencer, which provides the digital control signals for driving the front-end chip, and the clocks, both for the chip and for the
- DRAFT [3], a dedicated VME module designed to receive, decode and store the data from the ABC and ABCD chips;

- a CES VME Read–Out control board (CORBO) [4],
- a Lecroy 1176 Time To Digital Converter (TDC) and, finally,
- a Windows95–based data acquisition program.

The setup allowes to send software triggers and run the chip with the internal calibration circuitry, as well as receive an external scintillator trigger in the case of β–source tests. The main tests performed on the chip can be grouped in 3 sets: measurements on the chip with no detector bonded, measurements of chip electrical properties with a detector bonded and, finally, measurements with a β–source.

All the measurements were taken with the following bias conditions:

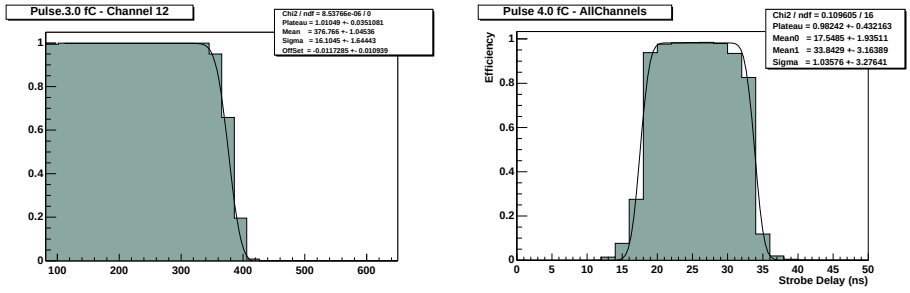
- Power supply: V_{dd} = 4 V, V_{cc} = 3.5 V
- Bias: I_{pream} = 220 μA, I_{shaper} = 19 μA

2.2 Results with no detector connected

The first set of measurements was made on a bare chip, with no detector connected at the input pads, and using the internal calibration pulse. A series of threshold scans and calibration strobe delay scans was made to compute the gain, offsets and time walk of the chip. For each channel and threshold scan a so–called s–curve was obtained. It represents the efficiency variation with the applied threshold for a fixed input pulse. For a calibration pulse, its shape should be that of a complementary error function:

$$\mathrm{scurve}(x) = \frac{1}{2} \times \mathrm{plateau} \times \mathrm{erfc}\left(\frac{1}{\sqrt{2}}\frac{x - \mathrm{mean}}{\mathrm{sigma}}\right) \tag{1}$$

The main parameters to be obtained from that curve are the 50% point or mean, that is, the value of the threshold at which the efficiency in the plateau drops by a factor 2, and the sigma of the associated gaussian, which is a measurement of the electronics' noise.



(a) (b)

Figure 2: *Example of a s–curve (a) and a time delay curve (b). In the threshold s–curve plot the parameters of the fit are shown. The one labeled as* mean *corresponds to the 50% point and* sigma *corresponds to the noise. In the strobe delay plot the parameters* Mean0 *and* Mean1 *are the points at which the efficiency in the plateau drops by a factor of 2 in both sides.*

The gain is computed as the slope of the straight line fitted to the 50% points of a given channel for different input charges. The offset will be defined as the ordinate in the origin for the fitted line.

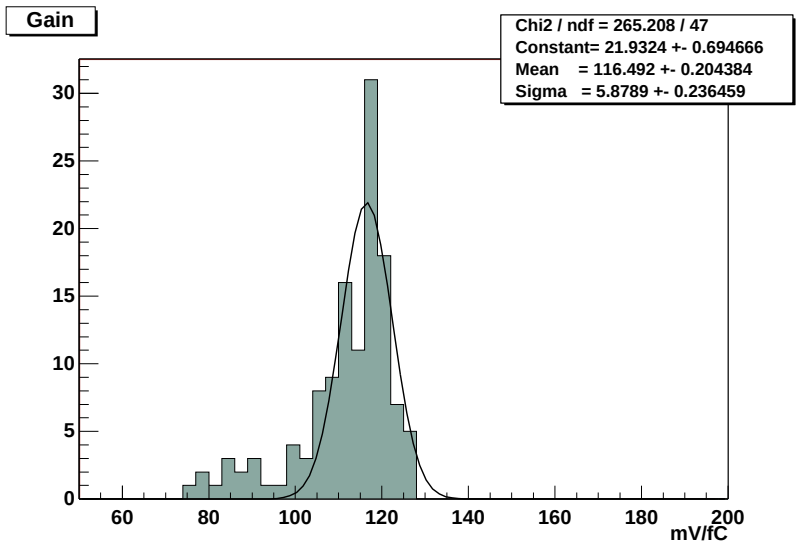


Figure 3: *Distribution of the gain across the chip for a bare chip.*

Fig. 3 shows the spread of the gain across the different channels in the chip. A value of 116.5 mV/fC is achieved, with a spread on the order of 6% across all the channels.

The noise spread across all the channels in the chip for a 3fC input pulse is shown in Fig. 4. An average value of 14.8 mV is obtained which, together with a gain of 116.5 mV/fC, gives an equivalent noise charge (ENC) of 790 e^- rms. In the same figure, the offsets across the channels are shown to peak at around -28 mV with a spread of 33.5 mV.

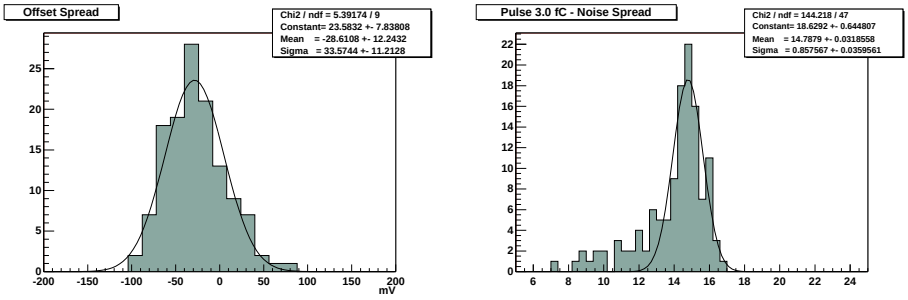


Figure 4: *Noise and Offset distributions across the chip when no detector is connected to the input pads of the chip..*

In order to measure the time walk, a scan is made on the calibration strobe delay for different calibration input pulses. For each channel and pulse height a curve like the one showed in Fig. 2.b is obtained and fitted to

$$\mathrm{TimeEff}\,(t) = \frac{1}{2} \times \mathrm{plateau} \times \left[\mathrm{erfc}\left(\frac{1}{\sqrt{2}} \frac{t - \mathrm{mean2}}{\mathrm{sigma}} \right) - \mathrm{erfc}\left(\frac{1}{\sqrt{2}} \frac{t - \mathrm{mean1}}{\mathrm{sigma}} \right) \right] \quad (2)$$

For every pulse, all the channels are summed up and a similar fit is done on the new curve. That will give the mean delay required for that pulse ($\frac{1}{2}\,(mean2 + mean1)$) to be efficiently registered, and the range in which all the channels have the maximum efficiency ($\frac{1}{2}\,(mean2 - mean1 - 4 \times sigma)$). Fig 5 shows the time walk curve which is made by subtracting the average delay of the highest pulse to the others and adding 10 ns offset to

stay further away from the falling edge of the curve. The vertical bars show the interval of maximum efficiency for a given pulse (see Fig. 2.b). A time walk of 12 ns for a 2fC pulse, with respect to a 16fC pulse, is obtained.

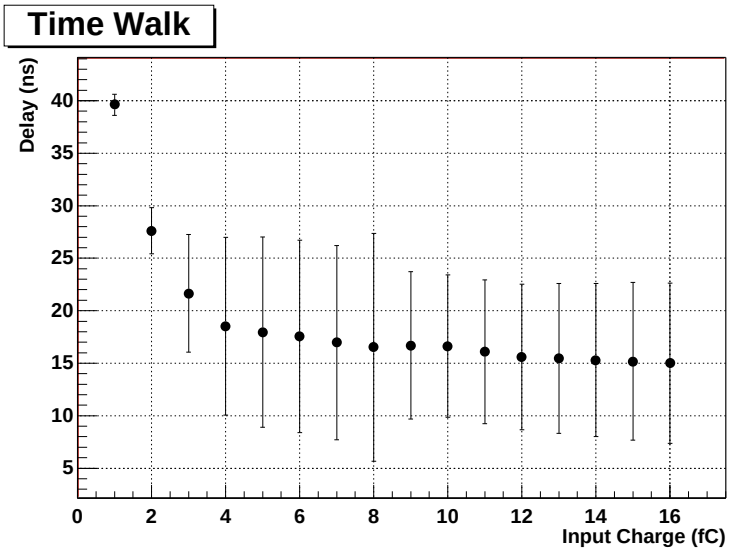


Figure 5: *Measured time walk with respect to a 16 fC input pulse. The vertical bars in the plot show the width in nanoseconds of the range of delays with maximum efficiency (see text).*

2.3 Results with $2\,cm$ detector connected

An 80 μm pitch, 2 cm long and 300 μm thick detector from SINTEF was bonded to the chip. The depletion voltage of the detector was 70 V but it was operated at 200 V in order to avoid ballistic deficit effects. In those conditions, the same measurements as in section 2.1 were made. Fig. 6 show the distributions for the gain, noise and offset of all the channels in the chip.

2.4 Results from a β source test

A ^{106}Ru source was used to test the chip performance with β particles. The ^{106}Ru source was masked with a plastic *collimator* to avoid large incicende angles of the β–particles in the detector. The setup for this mode of operation was still the same as described in section 2.1 but the system was triggered by the scintillator signal instead. A TDC was used to measure the relative delay between the scintillator trigger and the the T1 command sent to the chip. Fig. 7 shows the overall efficiency (chip efficiency and geometrical acceptance normalized to the number of scintillator triggers) as a function of that delay for a given threshold. The distribution was fitted with

$$\mathrm{TimeEff}\,(t) = \frac{1}{2} \times \mathrm{plateau} \times \left[\mathrm{erfc}\left(\frac{1}{\sqrt{2}} \frac{t - (\mathrm{mean1} + 25)}{\mathrm{sigma}} \right) - \mathrm{erfc}\left(\frac{1}{\sqrt{2}} \frac{t - \mathrm{mean1}}{\mathrm{sigma}} \right) \right] \tag{3}$$

where the width of the plateau is fixed to 25 ns.

Fig. 8 shows an indirect measurement of the chip walk time in the range of the signals produced by the ^{106}Ru source. The curve shows on the abcisa the values of the *mean* parameter obtained from the fits made for all the thresholds as a function of the threshold applied. The time walk is of the order of 10 ns.

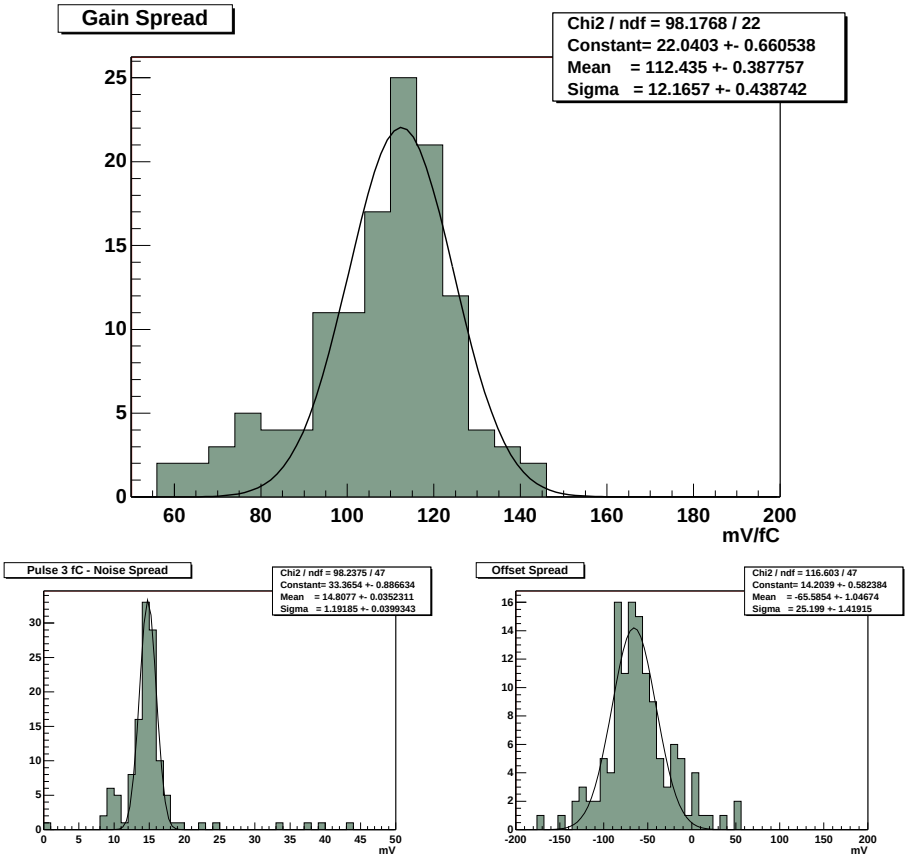


Figure 6: *Gain, noise and offset with a detector bonded. the detector bias was 200 V.*

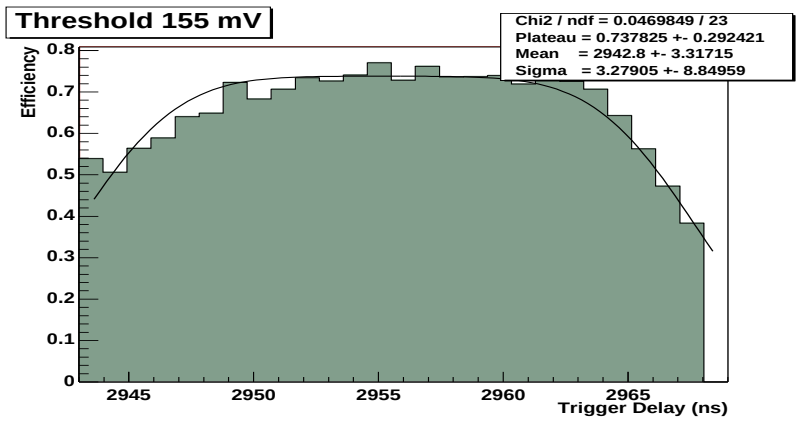


Figure 7: *Overall efficiency obtained with the β source as a function of the trigger delay for a given threshold.*

In order to obtain the s-curve, channels with hits were grouped in clusters which in turn were required to be *in time*, that is, the TDC value should stay in the region of maximum efficiency. Only events with one cluster were selected. Fig. 9 shows the s–curve obtained from the threshold scan for both modes of operation of the chip –edge and level mode– with a detector bias of 200 V. The curves are fitted to the convolution of a Landau distribution with a gaussian. Superimposed is the Landau distribution obtained from the fit for each one of the modes, with the vertical scale magnified in order to make it visible. The values in the vertical axis are a rough estimation of the overall efficiency (chip efficiency and geometrical acceptance). Assuming that for a 300 μm thick detector the maximum of the landau distribution corresponds to a charge of 3.5 fC and that the chip has an average offset of -65 mV (see Fig. 6), we obtain a gain of the front–end of 92 mV/fC for edge mode and 99 mV/fC for level mode.

The difference in gain between both modes of operation is due to the fact that some fraction of the signals with small orverdrive in the discriminator give slower responces which can be lost in edge mode. Apart from this, both modes give similar results.

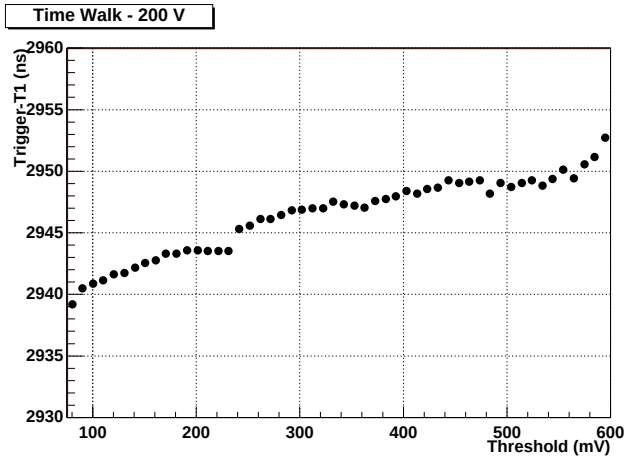
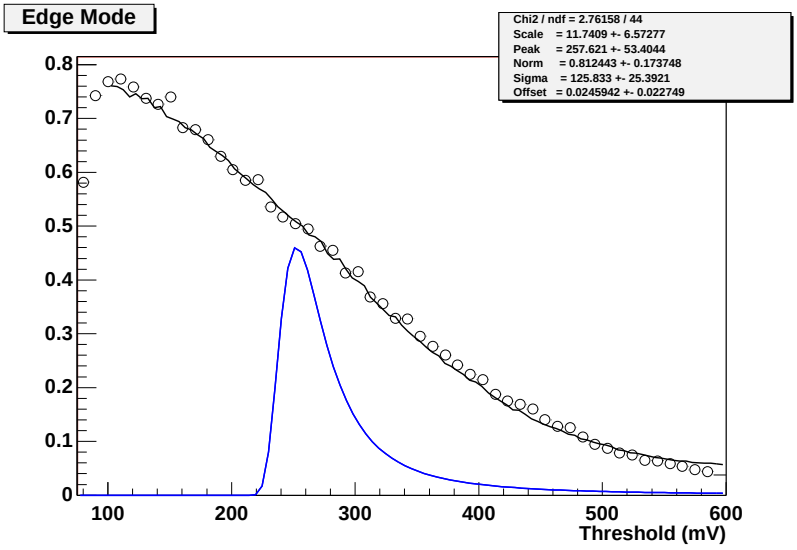
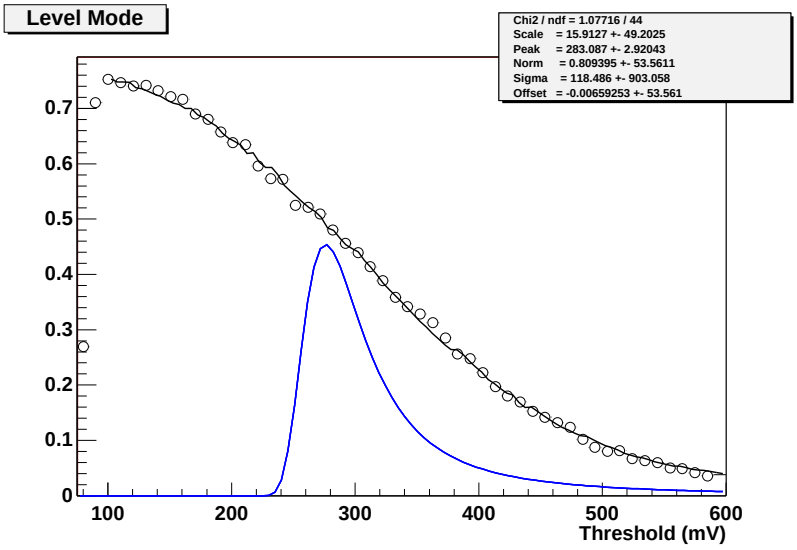


Figure 8: *Indirect measurement of the walk time of the chip for the signals produced by the β–source. It turns out to be on the order of 10 ns.*



(a)



(b)

Figure 9: *S–curves obtained in (a) edge mode and (b) level mode for a detector bias of 200 V.*

3 ABCD chips on hybrid

The ABCD chips have been placed on the ceramic hybrid developed by the Oslo group for the barrel module [5]. The hybrid, which can house 6 ABCD chips, plays the role of mechanical support, cooling and electrical readout. The hybrid circuit is printed using a commercial thick film process. The substrate is Beryllium Oxide (BeO). The results reported below will focus on the ABCD performances on the hybrid in comparison with the ones on the PCB already described in section 2.

3.1 Test setup

The setup used to check the ABCD's performance on the hybrid is shown in Fig.10. It basically consists of a VME crate which holds modules that provide the digital control signals and biases needed for the front-end chips and that are able to receive and store the data. One 4-wire power cable and one 50-wire flat&twist cable connect the VME modules to a support card designed by the Melbourne group [6]. The support card plays the role of mechanical support and provides the signals and biases to the hybrid via a kapton pigtail.

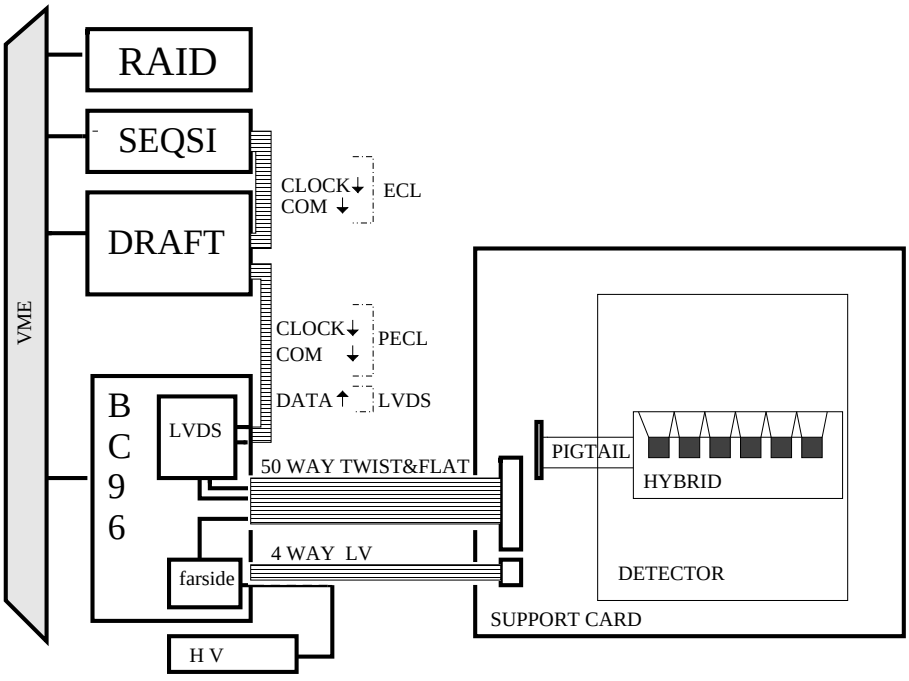


Figure 10: *Set up used for the ABCD test*

The VME modules used for the test are listed in the following:

- RAID: it is a VME board with a logical processing unit. The system test DAQ runs on it and the data are saved on its hard disk
- SEQSI: provides the digital control signals for driving the front-end chips (see section 2.1)
- DRAFT [3]: receives, decodes and stores the data from the ABCD chips (see section 2.1)

- BC96 [7]: it is a VME module that provides the voltages needed by the analog (VCC) and digital (VDD) sections of the front-end, routes digital control signals from the DRAFT to the support card via an LVDS driver (the ABCD needs LVDS control signals) and routes the digital data stream from the support card to the DRAFT.

3.2 Measurements and results

A number of measurements have been taken to check the performace of both the hybrid and the chips. The circuitry on the hybrid provides the following electrical functions:

- distribution of the clock and control to the binary pipeline circuitry,
- support of the redundancy functions of the digital chips and bypass lines for chip failures,
- return of the data to the off module optical transmission board,
- distribution and filtering of supply voltages to the front end chips.

All these functions have been succefully tested. However the following remarks should be added:

- The redundancy lines for the chip failures have been tested just in the case of a Slave Chip failure. The bypass logic, in case of a Master Chip failure, requires the connection of the first hybrid to a second one (double sided module) and therefore has not yet been checked.
- The final design with the optical data trasmission is not implemented yet, so the data trasmission has been succefully checked in the enviroment previously described.
- The default hybrid configuration has the analog ground (AGND) and digital ground (DGND) separated. However it is possible to connect them via a wire bond across two pads. The configuration with the two grounds connected together leads to much better results in the case of a complete module.

Two hybrids (Hyb1 and Hyb2) have been fully populated with ABCD chips with a major difference: on Hyb1 the backplane of the chips is left floating while on Hyb2 it is connected to analog ground. The aim is a comparison between the chip perfomaces in the two cases. Experience with the analog chip manufactured in the DMILL technology indicates that grounded backplane is a preferable solution which improves the stability of the front-end. Since the chips are not metallized, conductive glue has been used to place the chips on Hyb2.

In order to evaluate the chip performances, measurements were performed on the gain at the discriminator input, the noise at the discriminator output and the threshold uniformity across the 128 channels of a single chip. The internal DACs were used to control both the differential voltage for the discriminator threshold and the amplitude of the calibration signal. VCC and VDD are set at the nominal values (VCC=3.5 Volts and VDD=4.0 Volts). The input transistor current and shaper current setting is chip dependent (see A.1): they have been choosen in the range $193.2 - 211.6\ \mu A$ for the input transistor current and $19.2 - 22.8\ \mu A$ for the shaper current.

In Fig.11 it is shown a typical result from a threshold scan for 4fC injected charge for one chip. The 128 channels of the chip are superimposed. The S-curve shape is the expected one. Low efficiency at low threshold is due to the edge detection circuitry in the input stage: at low threshold the discriminator response is generated earlier and it can be latched to the previous clock. The spread of the S-curves indicates the main problem, i.e. a large spread of the discriminator offset across the chip.

The S-curves are fitted with an error fuction. The fit results, 50% values and σ, are plotted in Fig.12 for the 6 chips on Hyb1. The injected charge is 4 fC.

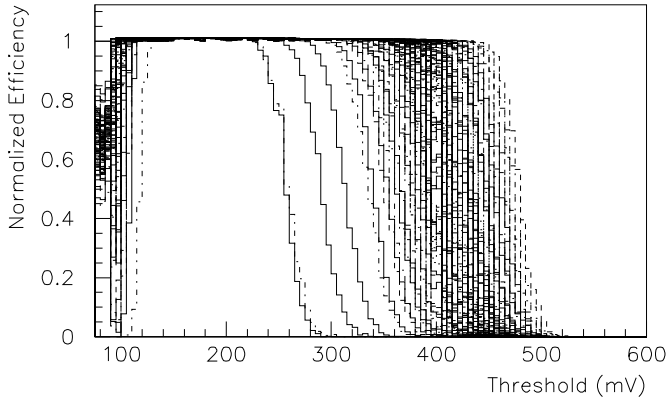


Figure 11: *S-curves from Chip 1 on Hyb1. The injected charge is 4 fC*

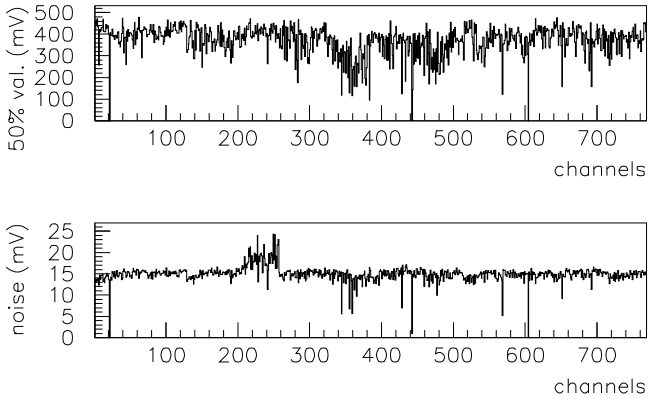


Figure 12: 50% *values and noise for the 6 chips on Hyb1 (768 channels)*

The gain at the discriminator input is calculated from a linear fit of the 50% values plotted as a function of the injected charge in the range of 2.0-4.0 fC (see Fig. 13).

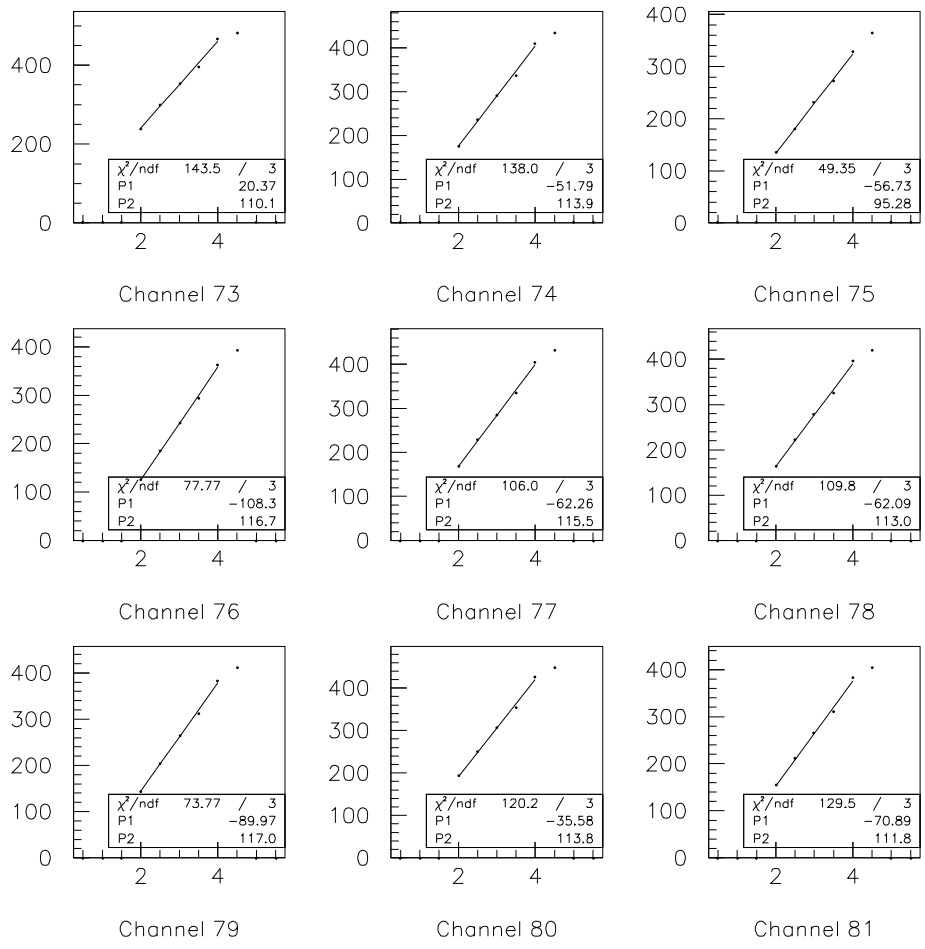


Figure 13: *Linear fit for 9 channels on Hyb1. P1 is the offset and P2 the gain*

Fig.14 and Fig.15 show the gain and offset distributions for the 6 chips on Hyb1 (some chips have less entries because of a cut on the χ^2 of the linear fit). A number of the channels have a large negative offset. This means that for charges smaller than 2 fC channels will be inefficient even for low thresholds. Moreover some chips show a saturation effect for charges greater than 4.0 fC, therefore the linear fit is performed over the range of injected charge of 2.0-4.0 fC. The gain is around 100 mV/fC for all chips with a variation of $\sim 4\%$ (1σ) in a single chip. The offset spread is very large for all chips (~ 40 mV) and it is out of the specifications.

Fig. 16 shows the ENC for the 6 chips. These values have been calculated taking into account the noise at 3.5fC instead of the one at 1fC (nominal threshold). The reason for that it is that for low charges, and so for low thresholds, there is some pick up from external interference. Therefore, in order to measure the physical noise generated by the front-end circuits, the noise at higher charge is more appropriate.

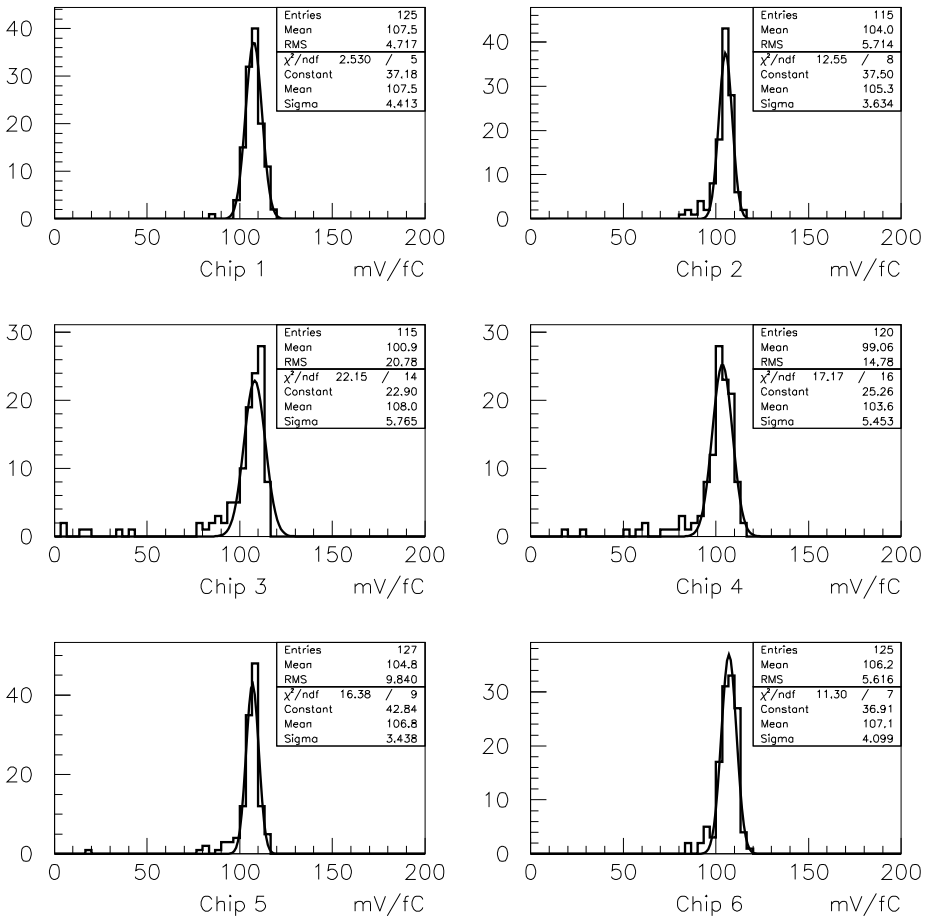


Figure 14: *Gain from the linear fit for the 6 chips on Hyb1*

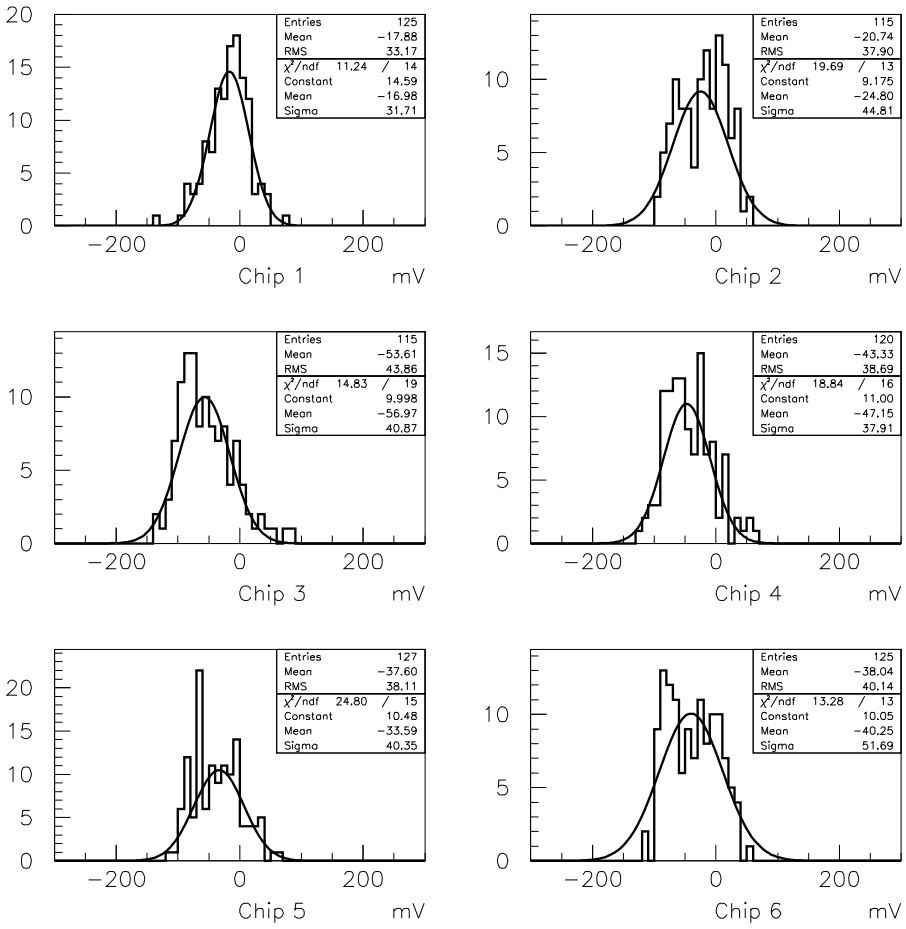


Figure 15: *Offset from the linear fit for the 6 chips on Hyb1*

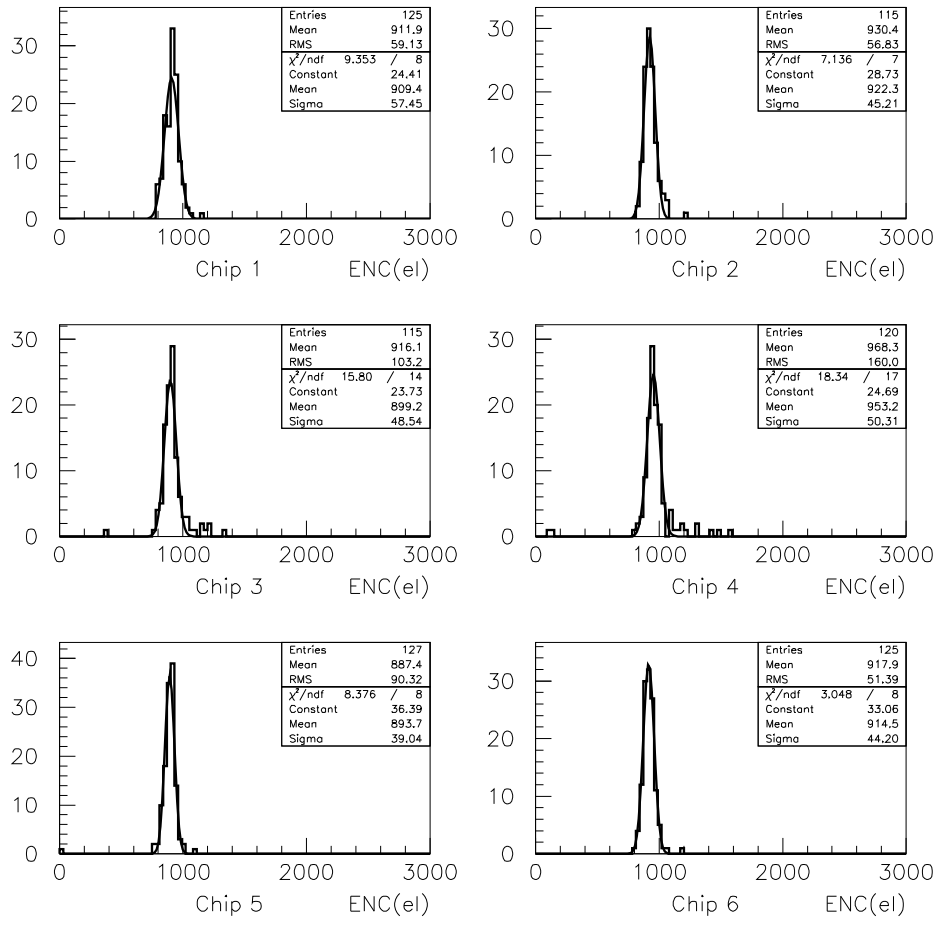


Figure 16: *ENC for the 6 chips on Hyb1*

The chips have a ENC higher than foreseen (900 electrons rms compared to the 625 electrons rms expected).

However if just a single chip is placed on the hybrid , the ENC gets much closer to the specifications. This means that the higher noise could come from common mode noise. It should be pointed out that the gain and noise distributions are based on the internal calibration circuitry, i.e. the calibration DAC and test capacitor. Given the absolute tolerances from the DMILL process parameters, we expect the obtained gain and noise to be accurate within $\pm 20\%$. An accurate calibration of the noise and gain will be possible only after a comparison with test beam data.

On Hyb2 we observe three chips having consistently lower noise ($\sim$ 700 electrons rms) compared to the remaining three. A possible explanation is that we obtained a good electrical contact with the backplane for those three chips while the contact was not effective on the remaing three. Given the fact that the backside was not metallized and not properly cleaned, the quality of the contact was not guaranteed at all. A hybrid with metallized chips will be built soon to resolve this uncertainty.

3.3 Module tests with silicon detector

Hyb1 and Hyb2 have been connected to silicon detectors to construct a complete single-sided module (Mod1 and Mod2 respectively). Each module consists of two 6 cm long strips silicon detectors glued on a ceramic baseboard, the hybrid and the support card. The strips of the two detectors are electrically connected to form 12 cm long strips. The detectors are CSEM silicon detectors of p-on-n type (p+ strips on an n-type bulk)[8]. The depletion voltage is 60 Volts while the total strip capacitance is approximately $20\ pF$. In the case of a complete module, the hybrid also provides filtering and DC current return for the detector bias line.

The basic parameters of the ABCD were measured with 12 cm long strips connected to the preamplifiers. The detector bias was set to 100 Volts to achieve full depletion. The test conditions and the data analysis were exatly the same used for Hyb1 and Hyb2. Our tests show that the hybrid configuration that minimizes the common mode noise is the one with DGND and AGND connected together. Results are reported in the following.

Fig.17 and Fig.18 show the gain and the offset distributions for Mod1. There is a remarkable deterioration of the chip performace. For a number of channels the gain drops by $\sim 20 - 30\%$ while in general the offset rms increases up to 70 mV.

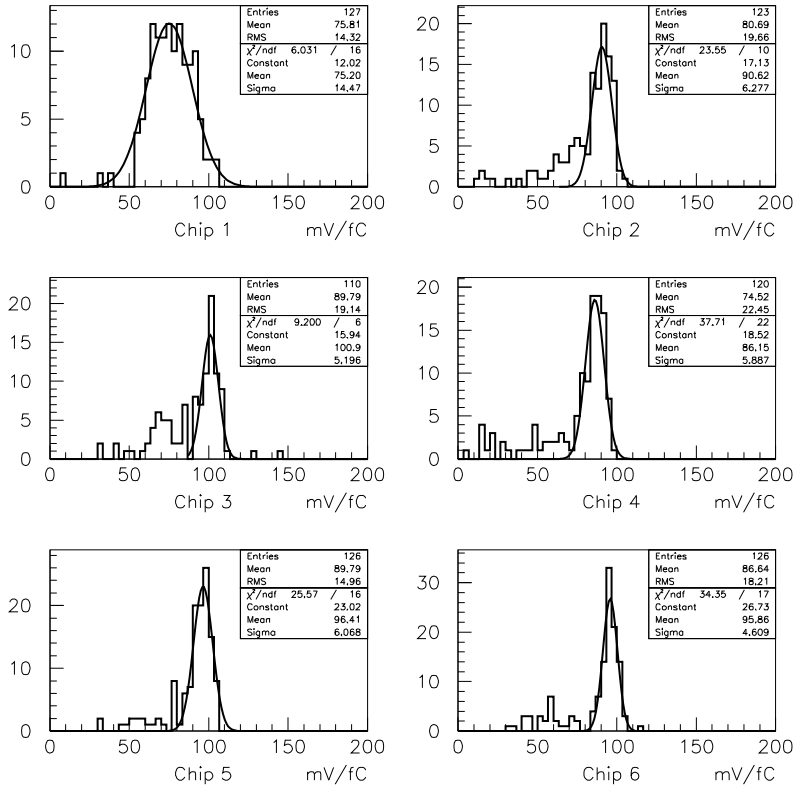


Figure 17: *Gain from the linear fit for the 6 chips on Mod1. The gaussian fit shows the peak value that is usefull for the comparison with Hyb1. However the gaussian function is not a good representative of the distributions*

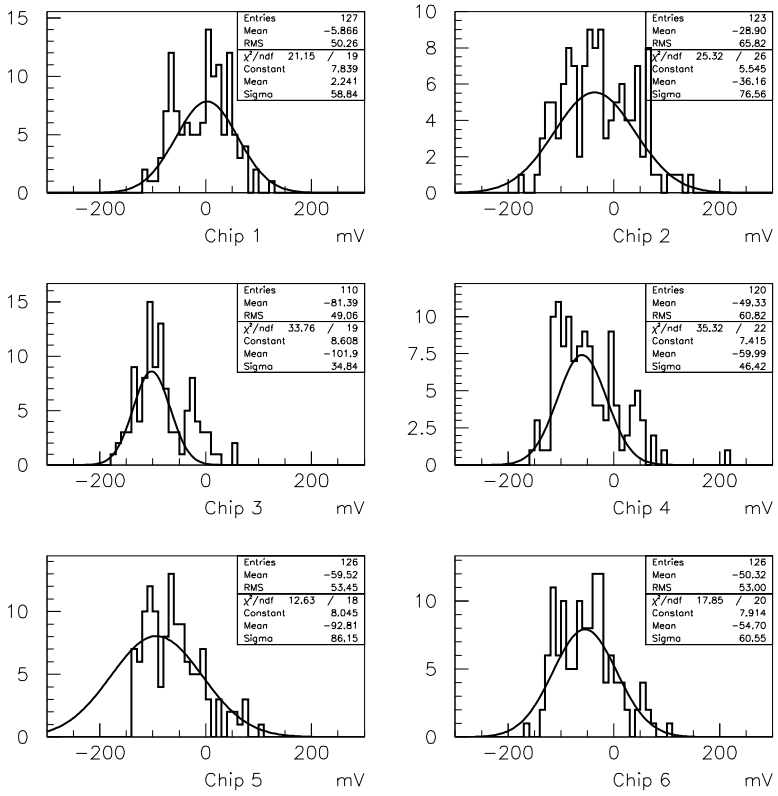


Figure 18: *Offset from the linear fit for the 6 chips on Mod1*

On average we observe an increase of noise from $\sim$ 900 electrons rms to 1600 electrons rms (see Fig. 19). Taking into account the total strip capacitance of $\sim$ 20 pF, this corresponds to a noise slope of $\sim$ 35 e^-/pF as expected from the design. A few channels on chip 6 were not connected to the detector. In fact for these channels the noise level was unchanged at about 900 electrons rms.

In order to measure the noise occupancy, the threshold scan without calibration pulse is performed. In this measurement only noise hits are collected. Figure 20 shows the noise occupancy plots for the 6 chips on Mod1. For each chip the average occupancy is shown. A noise occupancy of $\approx 10^{-5}$ remains even for high thresholds. This implies that there are high amplitude noise pulses which fire channels for any threshold.

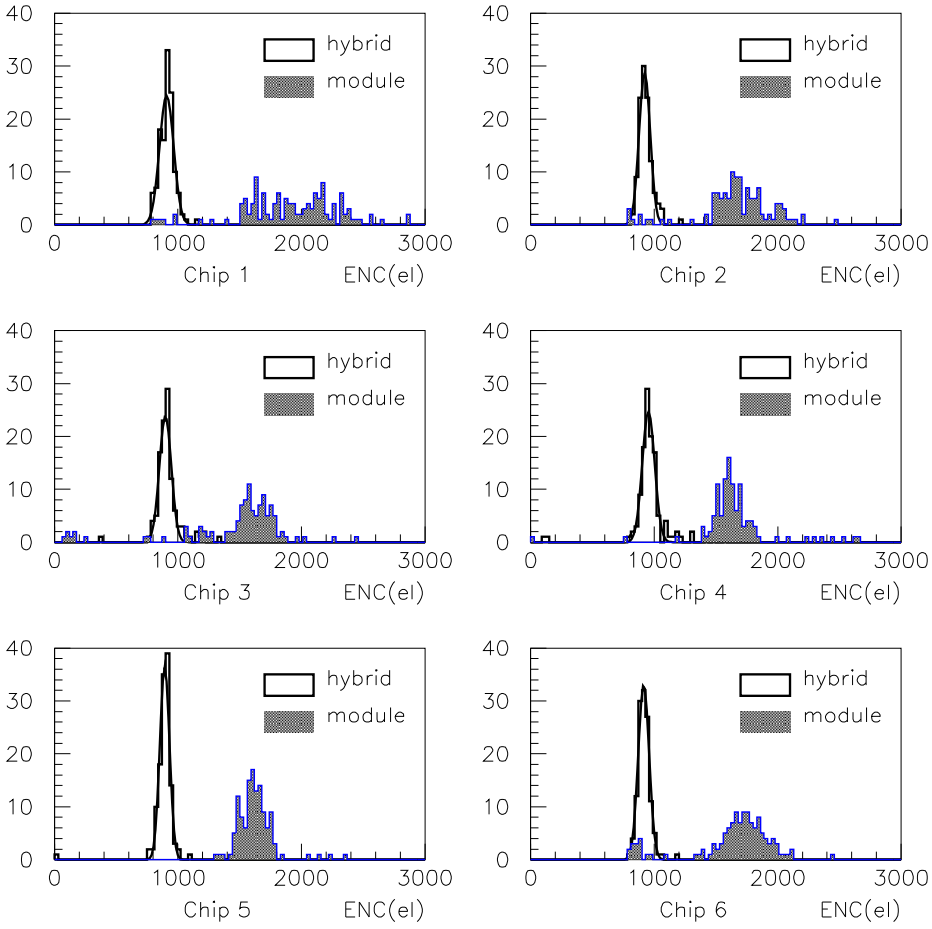


Figure 19: *ENC for the 6 chips on Mod1 compared to the one on Hyb1. Few channels on chip 6 are not connected to the detector. So these channels keep the noise level at about 900 electrons rms.*

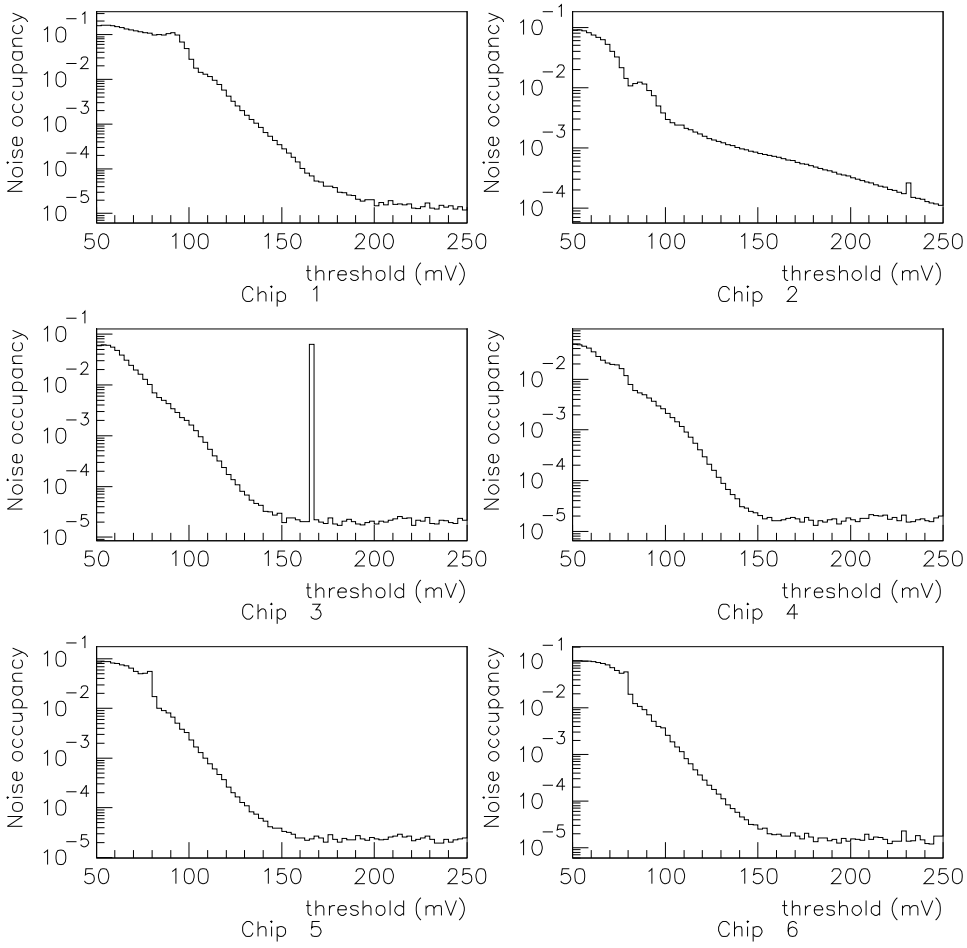


Figure 20: *Noise scan for 6 chips on Module 1. Note the logarithmic scale*

4 Conclusions

The results reported in this note show that the ABCD's digital part works satisfactory. The clock, commands and DACs can be loaded without problem. For the analog part, single chips meet the specifications for what concerns gain and noise performance. However the chip performance is deteriorated when attached to the hybrid: it has been shown that their performance depends on the hybrid configuration and is possibly affected by common mode noise. Anyway the major concern comes from the threshold non-uniformity among the 128 channels in one chip that is out of specifications.
In spite of the mentioned problems, the ABCD modules have been tested at Cern in the H8 beam line. They took succefully data during the period 20/8/98-26/8/98.

Acknowledgements

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A Problems

Here is a list of some problems that were faced during the test:

A.1 Front end parameters settings

According to the specifications, the ABCD chips should work for a wide range of the front-end settings namely 100-300 μA for the input transistor current and 10-30 μA for the shaper current. This was not the case for the analysed batch. In fact the process specifications were not fully met during the fabrication of this batch: the β is lower than the specified value and the resistors are at the high end of the specifications. The result is that the chip can operate only in a very narrow range of the bias settings. So, during the tests, the front end parameters working points were determined chip by chip. The paramenters depends not only on the chip itself but also on the number of chips placed on the hybrid and on the set up. A good set of parameters is the one that meets best the following requirements: stability of the front-end responce, high gain (around 100 mV/fC), low noise (less than 900 ENC) and uniform noise distribution along the channels. This problem should be solved in the next batch of ABCDs.

A.2 Low efficiency channels

Looking at the S-curve of some chips (see Fig.21), it is easy to spot that some channels never reach 100% efficiency even for low thresholds. A more detailed analysis of these channels show that for some of them it is possible to recuperate the lost events in the time slot following the triggered one, while for some others that's not possibile. Most likely the inefficiency of the second group of channels can have the following explanation: in the pipeline the data from each channel is multiplexed into 12 subchannels, each 12 cell long. If one of this twelve subchannels fails (e.g. it has one dead cell) then each 12th data for that channel is lost. As a result we get 91.6 % efficiency for that channel. For two or three subchannels broken we will get 83.3 % and 75 % efficiency respectively. This is compatible with the levels of inefficiency observed for these channels.

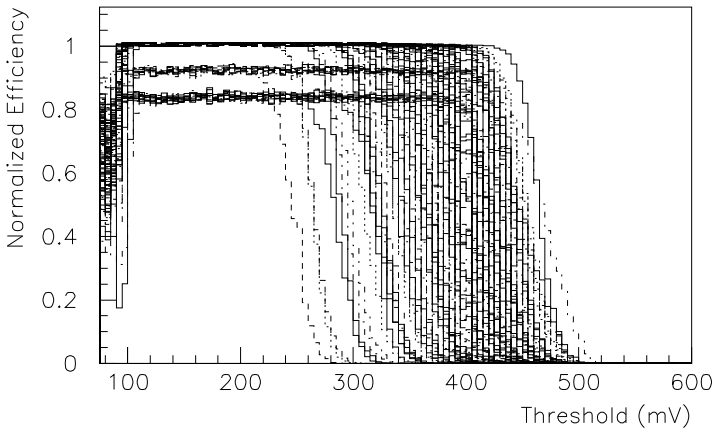

Figure 21: *S-curves from Chip 2 on Hyb1. The injected charge is 4 fC. Few channels never reach the* 100% *efficiency*

A.3 Trailer from the last chip

The ABCD internal logic requires that the logical level of $\mathrm{data_{in}} - \overline{\mathrm{data_{in}}}$ lines has to be "0" during the trailer transfer. If these lines are left floating, like on the last chip on the hybrid chain, the requirement may not be satisfied. In order to go around this problem the $\mathrm{data_{in}} - \overline{\mathrm{data_{in}}}$ lines's logical level should be forced to be "0" (for example they could be tied to VDD and DGND). This problem should not arise in the case of double-sided detector with two hybrids connected together and fully populated. However the revised ABCD design will solve this problem.

A.4 Gain analysis

As already explained, the gain analysis has been performed on the 2-4fC range. For some chips it is possible to extend this region to slightly higher charges. If this is done for the chips on Hyb1 (Hyb2 shows a clear saturation for charge greater than 4 fC), reaching 5fC, the result is a gain $\sim 5\%$ lower (and so the ENC$\sim 5\%$ higher), a big change on the absolute value of the offset ($\sim 50\%$) but no change on both the gain and offset spread. The big change on the offset value can be explained with the absence of values lower than 2fC. In addition the χ^2 of the fit over the range 2-5fC is slightly worst. In conclusion, the fit over the range 2-4fC seems to be more appropriate for the chips on Hyb1 and Hyb2. However the results from a fit over the 2-5fC region doesn't change the conclusion on the chip performances.

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