Electrical test results from ATLAS-SCT end-cap modules

Abstract

The LHC operating conditions present several challenges to the module performance of the ATLAS Semiconductor Tracker (SCT). This detector consists of four cylindrical barrel layers of silicon strip detectors and of 18 disks in the forward and backward direction. Four different module designs exist, one for the barrel and three (inner, middle and outer) for the rings of the disks. A series of several end-cap module pre-production prototypes of inner, middle and outer types have been built and extensively characterized on single module test benches in the institutes of the collaboration. The scope of this document is to summarize the electrical performance measurements made on these end-cap module pre-production prototypes, with special emphasis on the result of electrical tests after irradiation. As summarized in the conclusion, the electrical performance specifications are met before irradiation, but not after irradiation.

DRAFT

1 Introduction

The Semiconductor Tracker [1] (SCT) is one of the ATLAS Inner Detector elements which aim to track charged particles in the ATLAS experiment. It consists of four cylindrical layers (barrels) of silicon strip detectors, with nine disks in each of the forward and backward directions, permitting charged particle tracking up to a pseudo-rapidity of +/-2.5. Carbon fiber structures will support a total of 4088 modules, which are the basic functional sub-unit of the SCT. Each module consists of single sided silicon micro-strip detectors glued back to back with a 40 mrad stereo-angle, and attached to a hybrid. Both the detectors and the hybrid will be cooled during operation.

A fully assembled hybrid consists of a six layer copper-polyimide flex circuit, a substrate, SMD components (connectors, resistors, capacitors, a thermistor), twelve ABCD3T read-out chips [3], one DORIC and one VDC chip for the optical links. The ABCD3T is the final design of the single chip implementation of binary read out architecture, realized in the radiation-hard DMILL technology. It includes in a single chip all the blocks of the binary read-out architecture: the front end circuit, discriminator, binary pipeline, derandomizing buffer, data compression logic and the read-out control logic. The design and performance of these chips are mostly detailed in [3–6].

The SCT end-cap will be constructed with carbon-fiber disks covered by three kinds of modules - inner, middle and outer. Those types differ in the silicon detector dimensions. Outer and middle modules have an active strip length of 121.1 mm and 116.7 mm respectively while inner modules are formed with a single wafer of 72 mm length. The same hybrid is used for all three module types.

Eighteen end-cap module prototypes using the K5 hybrid version [2] have been assembled between February and November 2002 in several institutes of the SCT collaboration. Inner, middle and outer modules have been built and extensively tested electrically and thermally [17]. In this document, we will focus on the electrical performance of these K5 modules. The basic electrical requirements for SCT end-cap modules will be reported in the first section, followed by a description of the electrical test set up and a summary of the results obtained with the prototype modules. Some of the end-cap modules have been irradiated between May and October 2002 with the CERN PS 24 GeV proton beam, using the SCT T7 facility [18]: details on the tests performed will be presented.

2 Standard electrical module tests

2.1 Electrical requirements for the ATLAS-SCT end-cap module

LHC operating conditions result in very challenging performance specifications for the SCT modules and the limitations mainly concern the accepted noise and noise occupancy level, the tracking efficiency and the power consumption. The complete end-cap module electrical specifications are described in [1] and only the most important ones are reported here.

DRAFT

- **Noise performance**. The total effective noise of the modules results from two principal contributions, the front-end electronics and the channel-to-channel threshold matching. The former is the equivalent noise charge (ENC) for the front-end system (including the silicon strip detector parameters). It is specified to be less than 1500 e- before irradiation and 1800 e- after an irradiation of 3×10^{14} 24 GeV protons per cm^2. This noise hit rate needs to be significantly less than the real signal hit occupancy, to ensure that it does not affect the data trasmission rate, pattern recognition or track reconstruction. The foreseen limit value of 5×10^{-4} requires the discriminator level in the front-end electronics to be set to 3.3 times the rms noise. To achieve this condition at the ATLAS operating threshold of 1 fC, the total equivalent noise charge should never be greater than 1900 e-: assuming 3.3 fC median charge, that corresponds to a median signal-to-noise [1] ratio of 10:1.

- **Tracking efficiency**. In general the tracking efficiency of particle detectors is studied in test beams. Nevertheless, a starting requirement is a low number of dead readout channels, specified to be less than 7 for each module side to assure at least 99% of working channels.

- **Timing**. For a correct tracking reconstruction, every hit has to be associated to specific bunch crossing. That translates to a requirement on the timewalk of less than 16 ns, where the timewalk is defined as the maximum time variation in the crossing of the comparator threshold at 1 fC over a signal range of 1.25 to 10 fC. The fraction of output signals shifted to the wrong beam crossing is required to be less than 1%.

- **Power consumption**[7]. The nominal values for the power supplies of the ASICs are:

  · analogue power supply: Vcc = 3.5 V ± 5%;
  · digital power supply: Vdd = 4.0 V ± 5%;
  · detector bias HV, up to 500 V with a maximal leakage current of 2 mA [2].

  The nominal power consumption for the chips is foreseen to be 4.75 W during operation at 1 fC comparator threshold with 1% occupancy and 100 Khz trigger rate (L1 rate). Including the optical readout and the detectors, the total power dissipation should be less than 7.0 W per module.

- **Double pulse resolution**[8]. The double pulse resolution directly affects the efficiency. It is required to be 50 ns, to ensure less than 1% data loss at the highest design occupancy.

2.2 Set-up description and characterization tests

Standard electrical tests aim to verify the hybrid and detector functionality after the module assembly and to demonstrate the module performance with respect to the required electrical specifications.
The system used to perform electrical tests and data acquisition includes the following VME units (see figure 1):

[1] The S/N ratio mentioned here concerns the median charge as signal, contrary to another often quoted quantity that is the most probable signal; it corresponds to the peak value of the energy deposition distribution.
[2] to be checked ....

DRAFT

- a Multi-channel Semiconductor Tracker ABCD Readout device (MuSTARD[9]) to receive, store and decode data from the module;
- a SLOw command Generator (SLOG[10]) that allows the generation of SLOW commands for the control and configuration of ATLAS SCT Front-End chips;
- a CLOck And Control module (CLOAC[11]) that generates the clock, fast trigger and reset commands for the SCT modules , in the absence of a Timing, Trigger and Control system;
- a low voltage power supply[12], for the digital and analogue part of the chips (Vdd and Vcc);
- an high voltage supply[13], to bias the module detectors up to 500 V.

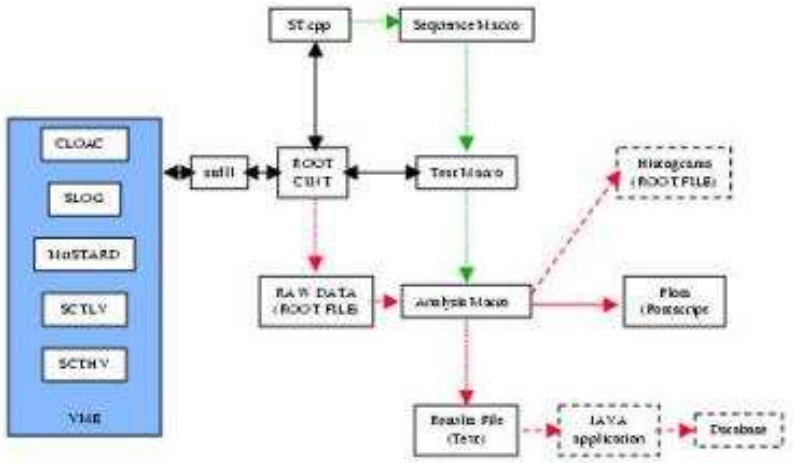

Fig. 1. Schematics of SCTDAQ system.

The DAQ software is a collection of C++ libraries (SCTDAQ) used together with the ROOT package: raw data acquired in each test are analysed by single root macros and stored in a database.
A single module is characterized to check the functionality and performance stability, and to verify if the specifications are met. Using the internal calibration circuit of the ABCD chips, the front end parameters such as gain, noise and channel-to-channel threshold spread are measured. The characterization procedure is described in detail in [14] and here a short summary is reported:

- digital tests are executed to identify chip or hybrid damage;
- an optimization of the delay between trigger and signal is performed on a chip by chip basis;
- to minimize the impact of the threshold non-uniformity across the channels on the noise occupancy, the ABCD3T design foresees the possibility to adjust the discriminator offsets. A threshold correction using a digital-to-analogue converter (Trim DAC) per channel with four selectable ranges, has been implemented in the ASICs [16]. The so called *trimming* procedure allows an improved matching of the discriminator thresholds; this is an issue especially for irradiated modules, due to the increasing of threshold spread with radiation dose;

- the gain and electronic noise (ENC) are obtained channel by channel with threshold scans performed with 10 injected charges in a range from 0.5 to 8 fC (ResponseCurve procedure). For each charge injected, the corresponding value in mV is extracted as the 50% point of the threshold scan fitted with a complementary error function (s-curve). The gain, input noise and offset are deduced from the correlation of injected charge in fC versus the voltage output (mV);
- a threshold scan without any charge injection is performed to yield a direct measurement of noise occupancy at 1 fC.
- to determine the timewalk a dedicated scan is also executed: setting the comparator threshold to 1 fC, for each value of injected charge (over a range of 1.25 to 10 fC), a complementary error function is fitted to the falling edge of a plot of efficiency vs. the setting of the delay register, to determine the delay at which the efficiency is 50%. The timewalk is given by the difference between delays calculated for 1.25 and for 10 fC charge injected.

The endcap prototype modules are tested in custom designed aluminium boxes which provide mechanical support as well as cooling. In these boxes, the modules are mounted on two aluminium surfaces, one beneath the hybrid, the other one at the far end of the detectors. Both surfaces are cooled with an alcohol-water mixture provided by a Huber chiller.

3 Calibration factor and temperature dependence

Two types of corrections have to be taken into account to compare modules with each other and with the real SCT conditions in ATLAS. First, the module characterization uses a calibration circuit that generates a voltage step pulse which is coupled to the front-end via a calibration capacitor (Ccal). To take into account variations of the capacitance from the design value, indirect measurements of this capacitance is performed during the ASIC wafer tests: table 1 shows the correction factor (C.F.) that must be applied in order to compare modules with each other. The real (corrected) gain and noise ENC are then given by:

$$\text{Real gain} = \text{Meas. gain}/\text{C.F.}; \qquad \text{Real ENC} = \text{Meas. ENC} \times \text{C.F.}$$

The second important correction concerns the temperature at which the measurements are made. The goal during SCT operation is to provide the most beneficial temperature conditions for positive annealing of the silicon detectors. Therefore the aim is to cool the detectors to -7°C in nitrogen atmosphere, using a two phase evaporative refrigerator cycle system, based on C_3F_8. Following simulations performed on the thermal conditions for the SCT, this corresponds to a temperature around +2 °C on the hybrid, measured by a thermistor placed on it.
To make electrical test results performed in the laboratory comparable with each other and with the real experiment conditions, front-end parameters sensitive to the temperature, such as gain and ENC noise, need to be normalized. Unirradiated modules are usually tested in an atmosphere at room temperature and are cooled with a liquid mixture at +15 °C provided by a chiller: the measured thermistor temperatures were in a range from 30° to 40 °C. For irradiated modules a cold environment is necessary to keep the detector temperature and consequently the leakage current reasonably low. A climate chamber set to -7 °C has been used to host the module, in

DRAFT

Module	*Cal. factor*	*Module*	*Cal. factor*
K5 300 (M)	1.093	K5 310 (O)	1.113
K5 301 (M)	1.093	K5 312 (O)	1.113
K5 302 (O)	1.150	K5 313 (I)	1.095
K5 303 (O)	1.171	K5 314 (I)	1.150
K5 304 (I)	1.171	K5 316 (I)	1.150
K5 305 (O)	1.171	K5 501 (O)	1.03
K5 307 (I)	1.150	K5 502 (O)	1.03
K5 308 (O)	1.095	K5 503 (O)	1.03
K5 309 (O)	1.113	K5 504 (O)	1.03

Table 1
Calibration factors as measured in wafer tests. The 12 ASICs mounted on a single hybrid come from the same wafer and are supposed to have the same calibration factor, so that a global correction to the module can be applied.

addition to the chiller set to -16 °C (effective coolant temperature ∼ -14.5 °C). Measurements

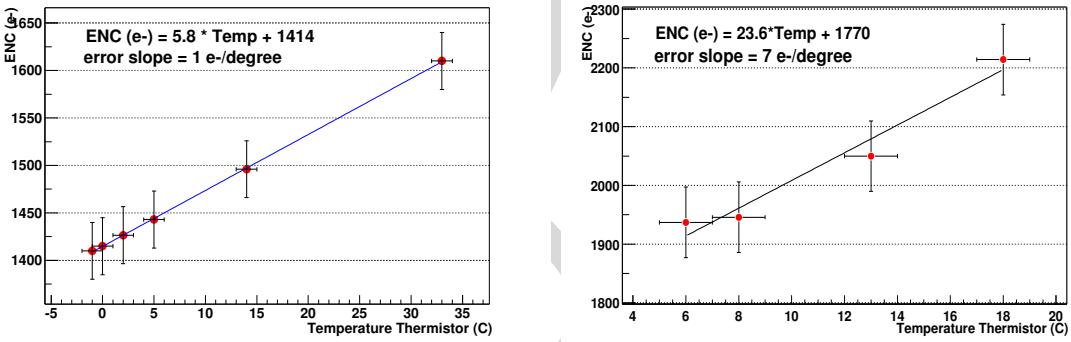

Fig. 2. *Left*: Temperature dependence of the noise is 5.8 $e^-/°C$ for an unirradiated outer module (ambient temperature at about +20 °C, V_{bias} = 150 V). *Right* The same plot for an irradiated module with ambient temperature at - 7 °C and constant V_{bias} = 350 V: the slope extracted from a linear fit is ∼24 e^-/°C.

performed on outer unirradiated modules (see figure 2) show the correlation between noise and thermistor temperature which can be fitted linearly with a slope of 5.8 e^-/°C. Since the temperature dependence of the noise is related to the strip capacitance, similar measurements have been performed for unirradiated inner modules, that lead to a correction of about 4.7 e^-/°C (see figure **??**).

The low accuracy both in the measured noise (ENC error estimation [3] ∼ 30 e-) and in the thermistor temperature (T error ∼ 1°C) lead to an error on the slope of ∼ ± 1.0 $e^-/°C$.

[3] The error quoted is an estimation of the statistical error, to be checked.

DRAFT

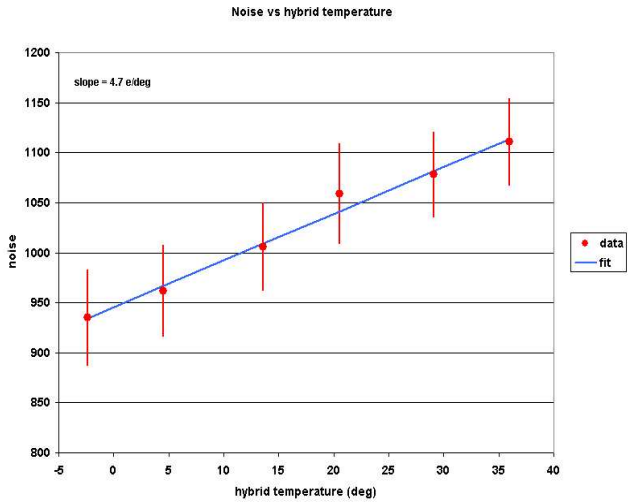

Fig. 3. Temperature dependence of the noise for an unirradiated inner module at $V_{bias} = 150$ V.

For outer irradiated modules [4], the study has been performed using a constant temperature of -7°C for the environment. In this case the slope of a linear fit results in a temperature dependence of the noise around 24 $e^-/°C$ [5] with an uncertainty of $\pm$ 7 $e^-/°C$, due also to the large error on the ENC values ($\pm$ 60 e^-)

4 Results from electrical tests of non-irradiated modules

A total of eighteen modules have been tested during 2002 in all the involved institutes: table 2 summarizes the front-end parameters as measured for the non-irradiated modules. It should be noticed that the outer module type corresponds the least favorable case in terms of noise, due to the higher contribution of longer detector strips ($\simeq$ 1500 e^- ENC noise to be compared to the $\simeq$ 900 e^- for the inner module).
The average module gain is about 49 mV/fC, corrected for each module with the appropriate calibration factor; using this correction and normalizing to the SCT temperature, the ENC noise in all outer modules is about 1440 e^-, while the average for the middle and the inner are 1345 and 925 e^-, respectively. In addition, the table reports the channel-to-channel threshold spread at 1 fC: matching of the gain and offset is a critical issue for a binary architecture and the non-uniformity acts as an effective contribution to the noise. The occupancy due to the effective

[4] A couple of words should be added to explain the uncertainty on the correlation also in comparison with other measurements:
- not possible to estimate the contribution of detector noise in changing the thermistor temperature;
- high sensitivity to the time of module biasing (a noise decrease is visible even after 24 hours);
- the module used for the measurement was only half-irradiated k5-310.
New measurement to be performed on k5-503 fully irradiated as soon as possible.
[5] The temperature correction actually used in the tables is still 15 e-/deg. measured on K3 irradiated module; this correction will be updated with new results.

noise at 1 fC is summarized in the last column of table 2 (see also figure 4). The column labeled as *corr* indicates the noise occupancy values corrected for the calibration capacitance variation and for the temperature, as mentioned in section 3. This correction was performed by fitting the occupancy as a function of the threshold, by a complementary error function, assuming that the noise is purely gaussian,

$$NO(t, ENC) = \frac{1}{2}\,\mathrm{erfc}\left(\frac{t}{ENC\sqrt{2}}\right) \tag{1}$$

where NO, ENC and t are the noise occupancy, ENC noise [6] and threshold values respectively. Inverting this complementary error function leads, for a given value of the noise occupancy, to a value of the ENC noise. This ENC noise is then corrected as specified above, and the corrected noise occupancy is obtained using once more the interpolation (1). It has to be noticed that the prototype hybrids have been equipped with non perfect – that is 1-dead channel – chips, except for K5 503 and 504, whose chips were perfect ones [7]. The unirradiated modules are well inside the requested specifications, having average noise ENC < 1500 e$^-$, noise occupancy below the foreseen limit 5×10^{-4} and efficiency in terms of working channel $> 99\%$. Figure 5 shows a representative timewalk scan. The typical timewalk that has been measured for unirradiated modules varies between 11 and 14 ns.

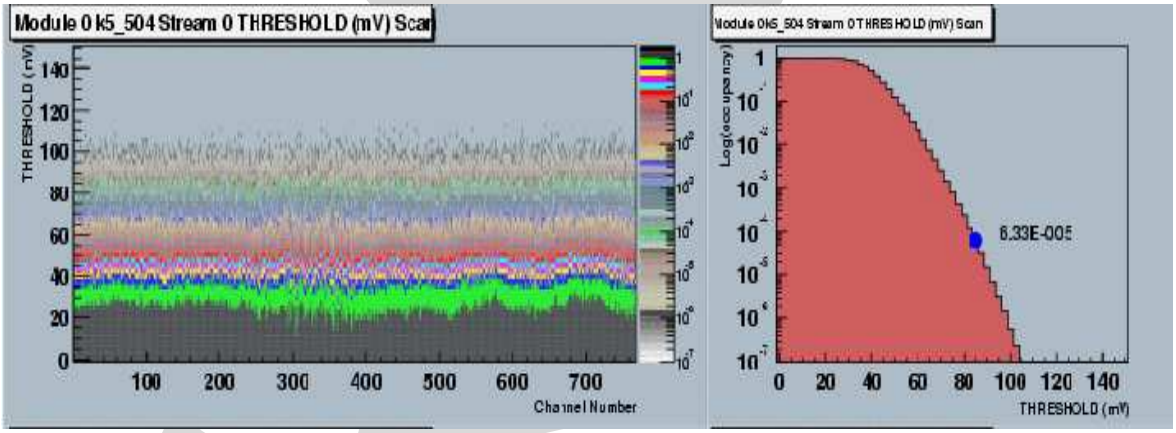

Fig. 4. Example of Noise Occupancy for the upper link of an unirradiated module: on the left hand side the 2D distribution of occupancy *vs* threshold per channel is shown, on the right hand side the projection of the occupancy in logarithmic scale for the whole link, that shows the expected shape. The dot indicates the 1 fC point as identified in the trimming procedure.

[6] It is worth noticing that this ENC value differs from that obtained by the response curve. The ENC deduced from the noise occupancy includes the contribution of both electronics noise and channel-to-channel variation. It therefore includes the threshold spread.

[7] About 20% of the production modules are foreseen to be equipped with 1-dead channel chips.

DRAFT

Module	*Gain*	*Thr. spread*	*T*	*Noise (e- ENC)*		*Occ.@1fC* $\times 10^{-4}$		*Masked*
	(mV/fC)	*@ 1fC (ENC)*	*(°C)*	*Meas.*	*Corr.*	*Meas.*	*Corr.*	*Chann.*
K5-300 (M)	47.8	167.0	38	1407	1340	0.13	0.06	0
K5-301(M)	50.1	160.0	40	1421	1351	0.15	0.06	10
K5-302 (O)	47.5	188.0	38	1419	1433	0.08	0.10	4
K5-303 (O)	48.1	206.5	33	1382	1447	0.03	0.10	8
K5-305 (O)	48.1	193.0	35	1393	1426	0.15	0.36	0
K5-308 (O)	47.1	182.2	47	1552	1445	0.40	0.17	4
K5-309 (O)	47.9	160.0	33	1435	1388	0.04	0.03	12
K5-310 (O)	48.1	143.6	31	1442	1413	0.20	0.20	0
K5-312 (O)	46.9	240.2	46	1524	1450	0.25	0.15	10
K5-501 (O)								
K5-502 (O)								
K5-503 (O)	49.3	152.6	39	1602	1436	0.43	0.09	2
K5-504 (O)	49.8	138.7	41	1634	1480	0.61	0.12	0
K5-304 (I)	51.5	118.0	44	1204	1212	$<10^{-7}$	$<10^{-7}$	1
K5-307 (I)	47.5	127.0	48	1276	1251	$<10^{-7}$	$<10^{-7}$	16
K5-313 (I)	50.5	150.0	44	1190	1106	$<10^{-7}$	$<10^{-7}$	10
K5-314 (I)	51.1	124.0	41	1134	1120	$<10^{-7}$	$<10^{-7}$	4
K5-316 (I)	51.8	142.0	42	1119	1099	$<10^{-7}$	$<10^{-7}$	4

Table 2
Module parameters as measured for unirradiated end-cap modules (middle, outer and inner). It is noted that K5-502, 503 and 504 have been tested on a prototype disk [15].

5 Irradiated modules

Seven of the modules have been irradiated at different fluences, with the 24 GeV proton beam of the CERN PS using the SCT irradiation facility. Four of them (K5 305, 308, 503, 504) have been irradiated with the nominal fluence of about 3×10^{14} protons/cm^2– simulating approximately 10 years of ATLAS operation. Two of them (K5-310, K5-303) have been irradiated to half the dose (fluence of about 1.5×10^{14} protons/cm^2). The remaining module (K5 312) has undergone a full irradiation in two steps: the first one was up to half the dose, and the second one four months later, to reach the total fluence [18]. We summarize in this section the electrical performance of these irradiated end-cap modules.

Unless otherwise specified, the measurements with irradiated modules were performed in a climate chamber with an environment at -7^oC. The modules are inside their test box with cold

DRAFT

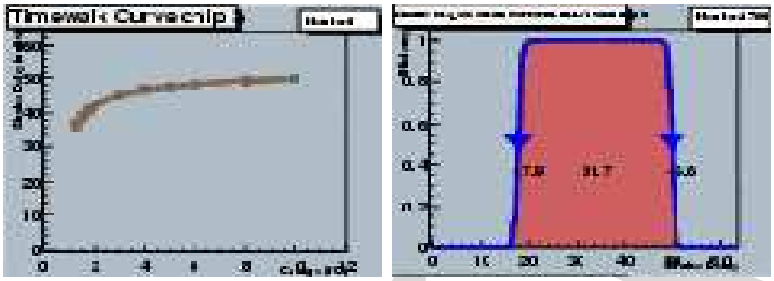

Fig. 5. Representative timewalk curves for one chip of an unirradiated module. *On the left*: for each injected charge, a chip by chip scan of efficiency vs. delay is performed to extract the 50% point of the falling edge. The corresponding delay (DAC units) is plotted vs. the injected charge and the timewalk is the difference between delay values at 10 fC and 1.25 fC. *On the right*: to convert DAC units to ns, the efficiency curve vs. delay (DAC units) is used. The width of the plateau, calculated as difference between the 50% point of falling and raising edge, should be 25 ns, so the conversion factor is extracted.

nitrogen flux; thermal grease is applied on both cooling points and the coolant, provided by a chiller, is at a temperature of -14.5^{o}C.

Radiations on silicon detectors induce both surface and bulk damage. The former is mostly due to an accumulation of charges in the interface between silicon oxide and the bulk; it affects for instance the interstrip capacitance, main contributor to the parasitic capacitance for the amplifier noise. The bulk is mostly damaged by displacement that leads to an increase of the leakage current proportional to the fluence and the silicon volume. Figure 6 presents the leakage current as a function of the bias voltage, with the hybrid unpowered. The curves are clearly consistent with the fact that irradiations have been performed at two fluences, since the leakage current is doubled in the case of a full irradiation with respect to the partial irradiation.

In addition to the damage of silicon detectors, the irradiation affects the front-end electronics. The ABCD chips are sensitive to ionization effects as well as to displacement damages. These contribute to a degradation of the current gain factor β of the input transistor, and consequently to an increase in the noise of the front-end; furthermore, the offset spread of the discriminator and the speed of the digital CMOS part are effected.

As consequence of the β factor degradation, the optimum values for shaper and preamplifier currents decrease; two 5-bit DAC implemented on the ASICs permit to change these values and the working point estimation is done checking different combinations of preamplifier and shaper current. Each chip can be independently adjusted and the front-end settings have therefore been re-optimized to obtain a high gain, but making a compromise to loose as few channels as possible. This procedure, the so called current scan, was done as the first step of the electrical tests, followed by the standard strobe delay and trimming test. For irradiated modules, the trim procedure is especially important, due to the increase in the ABCD discriminator threshold spread: more channels have to use large-range trimDAQ settings, where the correction step-size is more coarse.
The data presented are corrected both for calibration capacitor variation and for temperature, as explained in Sections 3 and 4. In Table 3 are displayed the gain, threshold spread, noise and

DRAFT

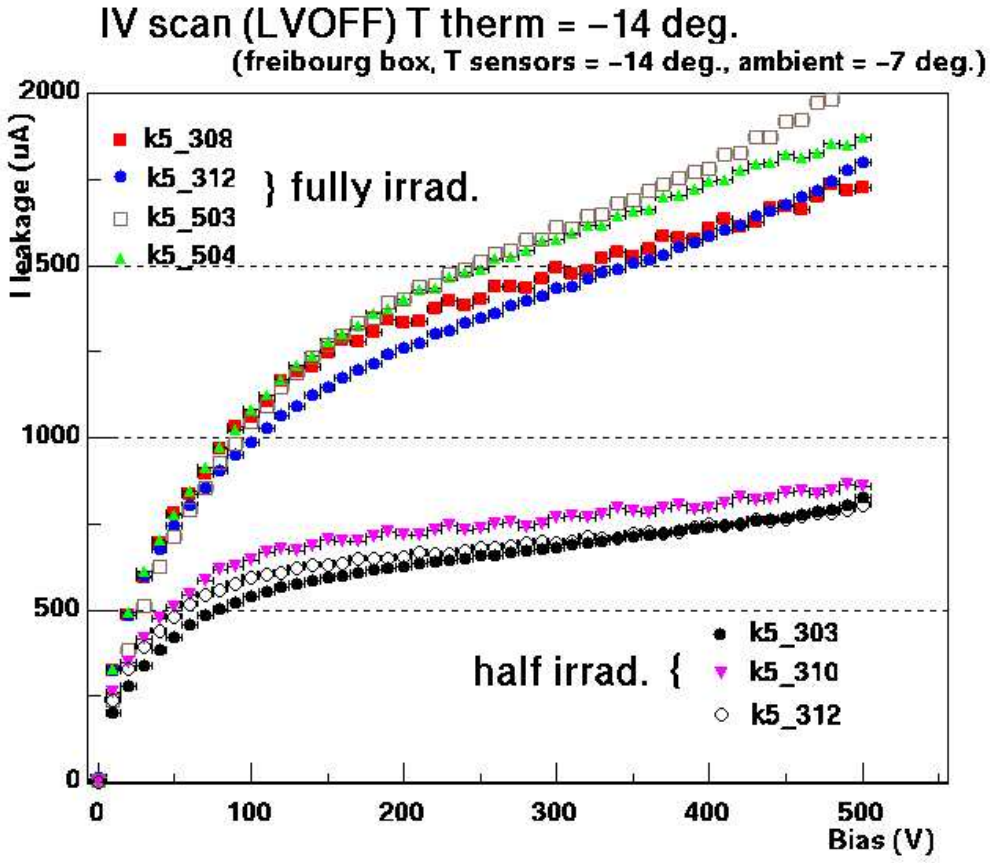

Fig. 6. Leakage current for half and fully irradiated modules.

noise occupancy of the half irradiated modules. Masked channels are also specified, since they have a direct influence on the module efficiency. No more than 1% of the channels should be lost on a module, which turns out to be satisfied by K5 303 and 312. However, K5 310 had one masked chip due to read-out problems.

Module	*Gain*	*Thr. spread*	*T*	*Noise (e- ENC)*		*Occ.@1fC* $\times 10^{-4}$		*Masked*
	(mV/fC)	*@ 1fC (ENC)*	*(°C)*	*Meas.*	*Corr.*	*Meas.*	*Corr.*	*Chann.*
K5-303	43.0	459.5	2	1528	1788	0.58	1.60	10
K5-310	37.0	479.2	7	1775	1882	5.03	9.10	43+128
K5-312	37.8	529.0	-1	1717	1938	3.31	13.80	16

Table 3
Front-end parameters as measured for half-irradiated outer end-cap modules. (Fluence $\simeq 1.5 \times 10^{14}$ protons/cm^2). K5 310 has a masked chip due to readout errors. The specifications are 5×10^{-4} for the noise occupancy, 15 masked channels at most, and an ENC not exceeding $1800e^-$.

As it can be seen in this table, the noise occupancy values are between 1.6×10^{-4} and 14×10^{-4} and ENC noise is between ≈ 1790 and ≈ 1940. Considering the fact that the luminosity will initially be lower, it can be expected from the previous results that the end-cap modules will reach the specification limits after about 7 years [1].

The front end parameters of the five fully irradiated modules are summarized in table 4. The noise level is between ≈ 2080 and ≈ 2400 ENC, and the noise occupancy between 20 and 90 $\times 10^{-4}$, while the specifications are 1800 ENC and 5×10^{-4} respectively. To reach the noise occupancy level required by the specifications, a threshold of 1.2 fC is thus necessary, as verified by plotting the noise occupancy distribution per channel (see Figure 8). Test beam analyses are then required to determine whether it is possible to use this threshold while maintaining the specified efficiency level [19,20].

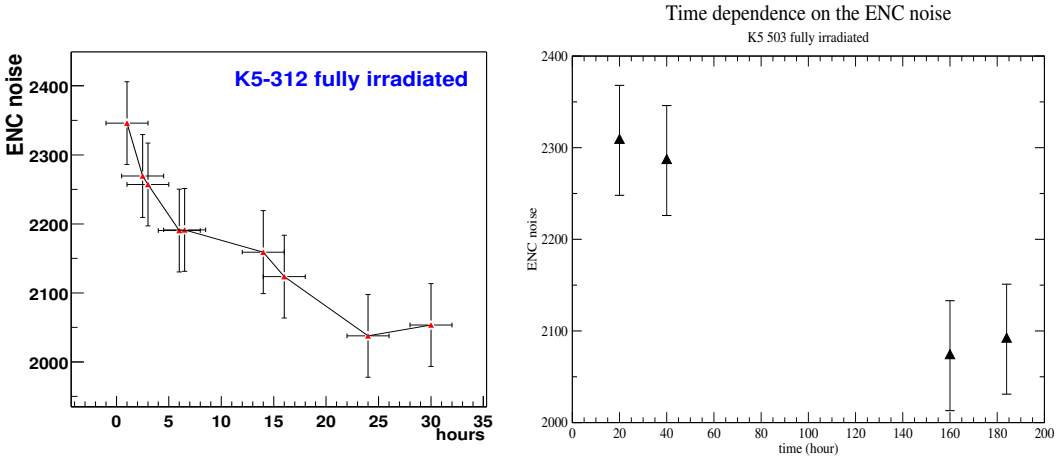

Fig. 7. Variation of the ENC noise with the time of bias for K5 312 (left hand side) and K5 503 (right hand side). The bias voltage is 500V.

ENC noise measurements have been performed on a long time scale to evaluate the dependence of the noise on the time of bias. The results are displayed in Figure 7 for K5 312 and K5 503, left biased at 500V. An ≈ 36 hours time scale study was performed with K5 312, while K5 503 has been biased during more than six days. It can be clearly seen from Figure 7 that the noise is decreasing very slowly. Between the first and the last measurement performed on K5 312, the ENC varies by more than 300 ENC. In addition, it is shown for K5 503 that even on a much longer time scale, the noise is still decreasing.

Module	*Gain*	*Thr. spread*	*T*	*Noise (e- ENC)*		*Occ.@1fC* $\times 10^{-4}$		*Masked*
	(mV/fC)	*@ 1fC (ENC)*	*(°C)*	*Meas.*	*Corr.*	*Meas.*	*Corr.*	*Chann.*
K5-305	27.6	614.0	1	2052	2408	54.80	88.00	7
K5-308	30.5	633.7	-1	1934	2156	27.26	63.50	5
K5-312	29.0	536.5	-2	1815	2077	5.33	21.20	20
K5-503	29.0	655.4	-6	2123	2307	46.92	80.70	29
K5-504	27.7	697.2	-5	2036	2202	40.50	68.60	17

Table 4
Front-end parameters as measured for fully-irradiated outer end-cap modules. (Fluence $\simeq 3.0 \times 10^{14}$ protons/cm^2)

DRAFT

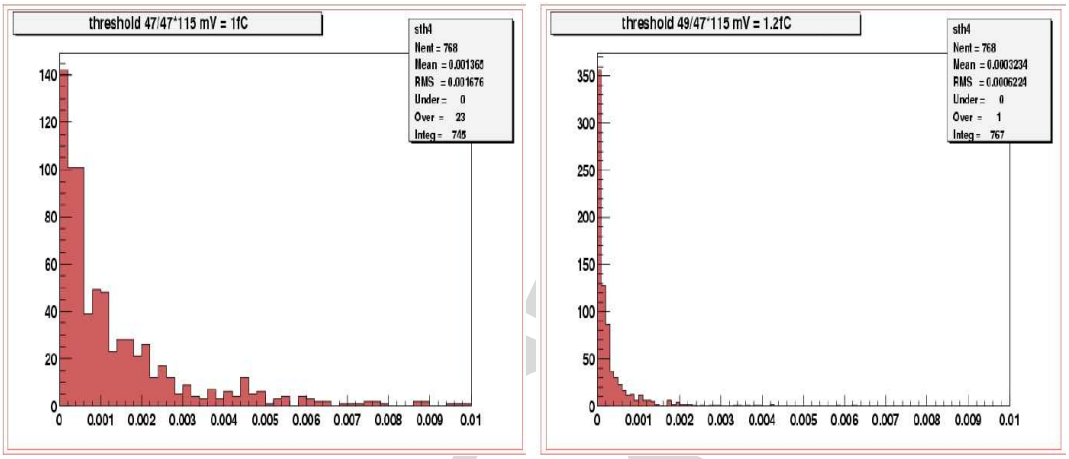

Fig. 8. Noise occupancy distribution of K5 503 (link0) fully irradiated, for two different values of the threhold discriminator: 1 fC (left hand side) and 1.2 fC (right hand side). Taking into account the outliers, not shown in these plots, the mean noise occupancy values are 9.10^{-3} and 5.10^{-4} respectively.

The time walk of fully irradiated K5 312, representative of the timewalk results for the irradiated modules, is displayed in figure 9. It shows a high number of channels with large timewalk: 746 channels out of the 1536 have a timewalk larger than the specification of 16 ns, and 11 being in another bunch crossing (that is above 25ns).

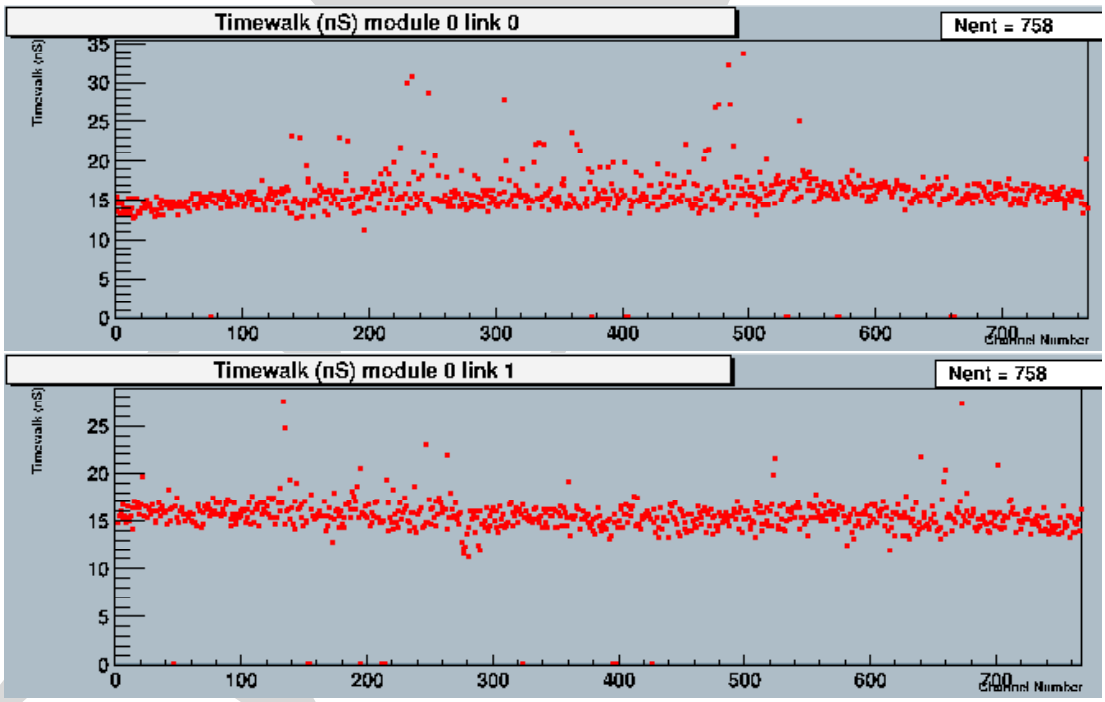

Fig. 9. Timewalk distribution of K5 312 fully irradiated, for link 0 and link1.

The degradation in timing performance is correlated with radiation effects in the analog part of the ABCD circuit. Modifying the digital power supply V_{dd} thus did not lead to any improvement of the timewalk. On the contrary, the high number of slow channels can be significantly reduced

by increasing the analog voltage, V_{cc}, supplied to the chips. The time walk profiles for V_{cc} = 3.5V and V_{cc} = 3.8V are compared in figure 10. Table 5 shows the influence of increasing V_{cc} from the nominal value of 3.5V to 3.8V by step of 0.1V. For this latter value, the timewalk distribution becomes flat across the chips and only 190 channels are above the required 16 ns, all of them having a timewalk less than 20ns. In addition to significantly reducing the discriminator

Vcc *V*	*TW>16ns* *# of ch.*	*TW>20ns* *# of ch.*	*TW>25ns* *# of ch.*
3.5	746	32	11
3.6	380	8	3
3.7	311	2	0
3.8	190	0	0

Table 5
Dependence of the timewalk as a function of the analog voltage V_{cc} of the chips. The results are given for module K5 312.

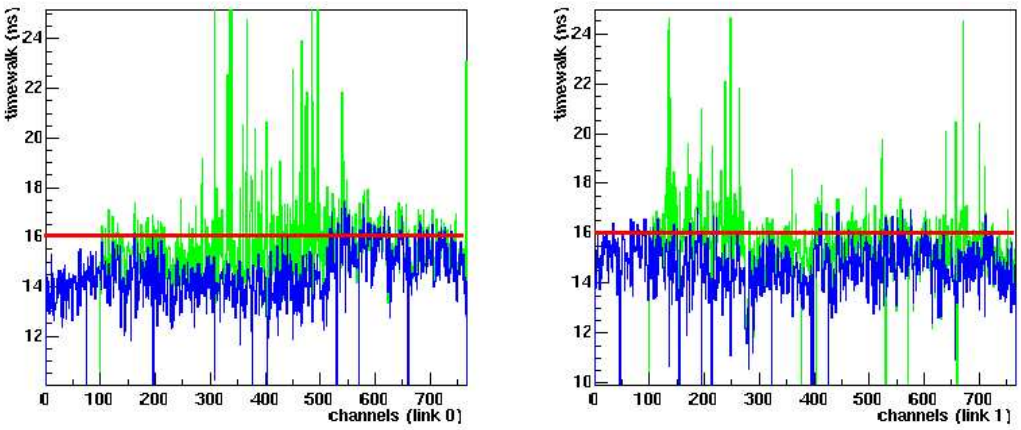

Fig. 10. Comparison of timewalk distributions across the channels (both sides) with V_{cc} =3.5 V (light line) and V_{cc} =3.8 V (dark line). The horizontal line corresponds to the specification requirement of 16 ns as maximal limit for timewalk.

timewalk for many channels, operating the ASICs at V_{cc} = 3.8V instead of the nominal value also slightly improves the front-end parameters, as can be seen in Table 6; in particular, the gain is on average 3 mV/fC higher and the noise occupancy is slightly reduced. It also allows the recovery of some channels, masked mainly because of the impossibility of being trimmed. However, the gain still remains non-uniform across the chips, as shown in figure 11.

The main issue in increasing the analog voltage when running irradiated modules concerns the power consumption of the module. This latter should not exceed 7W on the hybrid, and 1.5 W (2W) for the outer module wafers (inner module wafers) [21]. . Since the front-end bias currents of irradiated modules are smaller than the ones of non irradiated, the power consumption can be maintained within this limit, as shown in table 7, where the maximuml power consumption for all irradiated modules, for V_{cc} = 3.5V and V_{cc} = 3.8V, is evaluated.

DRAFT

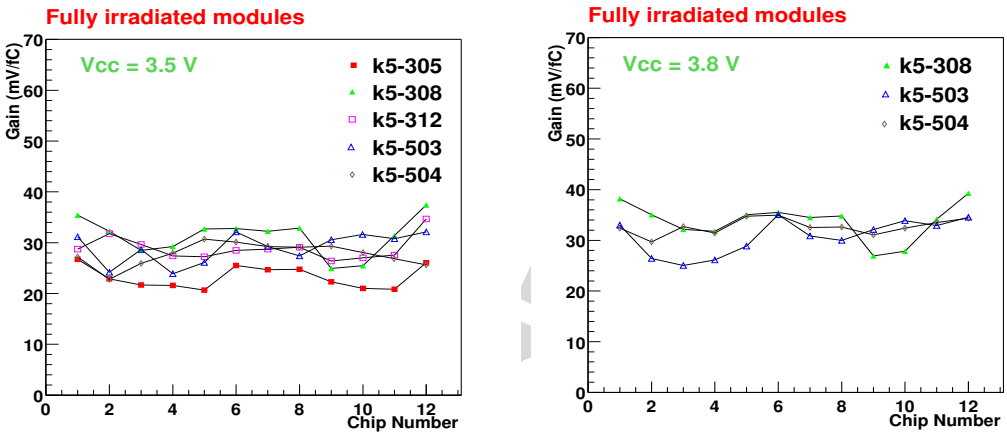

Fig. 11. Gain distribution across the chip for irradiated modules k5-308, 503 and 504 operating at V_{cc}= 3.5 V (left) and 3.8 V.

Module	*Gain* (mV/fC)	*Thr. spread @ 1fC (ENC)*	*Noise (e- ENC)*	*Occ.@1fC* $\times 10^{-4}$	*Masked Chann.*
K5 308	30.5/33.7	634/582	2156/2159	63./20.	5/5
K5 503	29.0/31.6	655/661	2307/2180	81./28.	29/12
K5 504	27.7/32.7	697/577	2202/2211	69 /40.	17/3

Table 6
Comparison of front-end parameters operating the modules with $V_{cc} = 3.5V$ or $V_{cc} = 3.8V$. The first (second) number of each column corresponds to $V_{cc} = 3.5V$ ($V_{cc} = 3.8V$)

6 Conclusion

The electrical performance of end-cap pre-production prototypes, has been described. Measurements were performed on single module test benches for all the three types of end-cap modules. Given the fact that up to eighteen modules have been studied, the results obtained are representative of the typical performance of the end-cap modules prototypes.

The non irradiated modules are well within the specifications, with a noise occupancy not exceeding 4×10^{-5} and a mean ENC noise of 1440 e^- in the least favorable case of outer modules. Two outer modules have been irradiated to the level of approximately 1.5×10^{14} protons/cm^2, corresponding to half the fluence expected during ten years of ATLAS life time. The noise then reaches values between 2 and 14 $\times10^{-4}$ and ENC noise between 1790 and 1940 e^-.

Five modules have been irradiated at the full dose, resulting in a noise occupancy level between about 90×10^{-4} and 20 $\times10^{-4}$, and an ENC in the range 2070-2410 e−, whether the specifications are respectively 5 $\times10^{-4}$ and 1800 e^-. The nominal noise occupancy limits would be met by increasing the threshold discriminator up to 1.2fC. Nevertheless, beam tests are required to confirm that such a threshold value could be used, keeping the efficiency (including masked channels) above the specified 99%. The characterization of these irradiated modules have been made over a period of several days, leaving the modules biased at 500V more than one day

DRAFT

Module	*Average*		*Maximal*		*Power Consumption*	
	Icc (V)	*Idd (V)*	*Icc (V)*	*Idd (V)*	*Aver (W)*	*Max (W)*
Vcc = 3.5 V, Vdd = 4.0 V						
K5-308	670	690	760	850	5.4	6.0
K5-312	620	810	680	950	5.1	6.2
K5-503	670	620	770	800	4.8	5.9
K5-504	660	640	760	830	4.9	6.0
Vcc = 3.8 V, Vdd = 4.0 V						
K5-308	710	680	820	870	5.6	6.7
K5-312	690	620	—	—	5.1	—
K5-503	700	610	750	840	5.1	—
K5-504	670	600	740	830	4.9	6.1

Table 7
Power consumption using the nominal Vcc = 3.5 V (on the top of the table) and Vcc = 3.8 V (on the bottom), keeping the digital bias at the nominal value 4.0 V. The maximum power consumption is calculated as $\mathrm{Icc}_{max} \times \mathrm{Vcc} + \mathrm{Idd}_{max} \times \mathrm{Vdd}$ (overestimate, maybe to be changed).

before starting the measurements, due to the time needed to reach the equilibrium. The ENC noise in particular sensibly decreases, over several days of bias (few hundreds of electrons). At the nominal value of the analog voltage of the front-end chips, many channels have a time walk larger than 16 ns., and a significant number are even in another bunch crossing. However, it is worth noticing that increasing the analog voltage from 3.5V to 3.8V reduces considerably the discriminator time walk for many of them, thus permitting the recovery of almost all channels. In addition, when operating the ASICS at this increased voltage, there is a slight improvement of the gain (3mV/fC) and the noise occupancy.

The SCT end-cap modules passed a Final Design Review in December 2002 and production is now starting.

References

[1] ATLAS TDR 5, Inner Detector Technical Design Report, Vol II, CERN/LHCC 97-17, April 1997.

[2] FDR

[3] W. Dabrowski et al., Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker, IEEE Trans. Nucl. Sc., Vol. 47, No 6, Dec. 2000.

[4] W. Dabrowski et al., The ABCD binary readout chip for silicon strip detectors in the ATLAS

DRAFT

Silicon tracker, Third Workshop on Electronics for LHC Experiments, CERN/LHCC/98-36, p.175-179.

[5] W. Dabrowski et al., Progress in the Development of the Read-out Chip for the ATLAS Semiconductor Tracker, Proceedings of the Sixth Workshop on Electronics for LHC Experiments (LED2000), Krakow, Sept. 2002

[6] ABCD Project specifications

[7] C. Lacasta, Electrical Specifications and Expected Performances of the End-cap Module, ATL-IS-EN-0008.

[8] ATLAS Note ATL-COM-INDET-2002-018.

[9] http://hepwww.rl.ac.uk/atlas-sct/mm/Mustard/MUSTARD.PS;

[10] http://hepwww.rl.ac.uk/atlas-sct/mm/Slog/SLOG.PS;

[11] http://www.hep.ucl.ac.uk/ mp/C-C Master regs+busy memo.txt

[12] to be added;

[13] to be added;

[14] P.W.Phillips,L.Eklund *Electrical Tests of SCT Hybrids and Modules.*

[15] System Test reference

[16] W.Dabrowski et al. *Radiation Hardness of the ABCD Chip for the Binary readout of silicon strip detectors in the Atlas semiconductor tracker.*

[17] K5 thermal note

[18] P. J. Dervan et al, Irradiation of ATLAS SCT Modules and Detectors in 2002.

[19] Test beam note

[20] Source measurements on K5 modules

[21] *Tests of Forward SCT cooling Blocks*

DRAFT