Minutes of the module electrical testing meeting, 21 July 2000

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Agenda:

10:30	Overview, scope, history	S.Roe
	Chip burn-in	Wladek Dabrowski
	Temperature cycling	(??)
12:30	Lunch	
14:00	Electrical test details	Peter Phillips
	CDF experience	Carl Haber
	Electrical testing	Nobu Unno
	Acceptance decision tree	(led discussion)
	Testing Hardware	(Gareth Moorhead / M.Morrissey?)
	Environmental factors	(discussion)

1. Overview, scope

http://sroe.home.cern.ch/sroe/Overview.pdf

The purpose of the meeting was to discuss a common standard for the hybrid and module quality assurance, with agreed electrical tests which include temperature cycling and burn-in conditions.

2. Chip burn-in

http://sroe.home.cern.ch/sroe/Burnin.pdf

It was emphasized that a proper assessment of effective burn-in times requires a statistical study of large numbers of chips, which is impractical in our case. Further, given that we will perform burn-in on hybrids and complete modules, there is a real risk of aging components unrealistically and causing failures (an additional graph was shown depicting the strong dependence of bond lifetime on temperature).
In the following discussion it was agreed among those present that we should keep with the currently projected burn-in scheme of **100 hrs at 50°C for the first batch of wafers, and aim to decrease this time for successive batches.** Each batch consists of 25 wafers, and the burn-in should be performed on the stuffed and bonded hybrids. The temperature of 50°C has been accepted as the maximum 'safe' temperature for such an operation, though it was noted that some hybrids have been subjected to 100°C without damage.

3. Temperature cycling

The EIA/JEDEC standard for temperature cycling was shown (http://sroe.home.cern.ch/sroe/TempCyc.pdf) by way of illustration of a 'typical' temperature cycling regime. Given that one of the purposes of temperature cycling is to catch poor surface mount joints by successive thermal stressing and relaxation, it was agreed that this was most usefully done at the manufacturer of the hybrids. Those present did not see a problem

in having the manufacturer perform temperature cycling for this purpose, before ASICs are mounted. With the ASICs mounted, the hybrid would simply be tested for functionality **at the operating temperature.** Further temperature cycling would later be performed on the completed module, by **cycling from –30°C to +50°C ten times**.

4. Electrical test details

http://sroe.home.cern.ch/sroe/Electric.pdf

A comprehensive series of tests were described divided broadly into a 'characterisation sequence' and a 'confirmation sequence'. The characterisation sequence is intended to be performed once on the hybrid, after burn-in, and once on the finished module. The confirmation sequence would be performed regularly during burn-in to check the functionality. Acceptance is defined for each series of tests in the document.

5. CDF experience

(no electronic version; summary below)
Carl reported on the CDF QA experience, with some detailed statistics. The CDF modules had 8 SVX chips plus digital transceiver , about 50 surface mount resistors, and 48 caps (6 tantalum). These were hand loaded with individual reflow.
Of 500 substrates tested, 425 were good (including those after rework).
265 were perfect from the outset, 160 were bad but 116 were repaired, having had bad bonds, wrong component or bad die (57 die replaced). 21 were cracked and 23 were difficult to repair.
All die were probed before and after dicing. All hybrids were burnt in for 48 hours, and 14 failed during burn-in.
Observations:

6. A two wire flying probe for hybrid testing would have been extremely useful.
7. SMT size 0402 are problematic: difficult to handle and to identify the value.
8. Good quality bond pads are critical
9. Wirebond heights were a problem (*specific to the SVX chip, I think*)
10. Fanout quality was variable.

6. KEK Electrical testing

http://atlas.kek.jp/~unno/prod/HybridModuleQAplan.fm52.pdf

Nobu presented a test programme for modules which was complete but different from what has been previously discussed as a testing baseline in the collaboration; S. Roe volunteered to summarise these differences and highlight points for further discussion with the aim of achieving some common agreement.

7. Acceptance decision tree

This was not discussed, pending an agreed testing sequence.

8. Testing hardware

http://sroe.home.cern.ch/sroe/hardware.pdf

Martin asked whether parametric testing was desirable on the hybrid, and if so explored the hardware possibilities for achieving this. In earlier discussions with Wladek (who was not present during this presentation) the opinion was expressed that parametric testing should only be done at the chip level.I t also seems that the chip testing hardware developed by H. Niggli can be used for parametric testing of hybrids if necessary, with little modification. This might be useful for occasional testing of irradiated hybrids (for example), but would not be foreseen for routine production testing of hybrids/modules.

9. Testing environments

The question of cleanliness in the testing environments was discussed. The point was made that the experiment itself would likely have a significant amount of dust inside, and the majority of people agreed (with one dissent) that while 'sensible cleanliness' should be maintained in the testing environment, there was no compelling evidence which would suggest we need class 10000 (or better) clean rooms for this purpose.