Silicon Detectors for Forward Tracking in ATLAS

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Abstract

A 12 cm long silicon microstrip detector module with a fan geometry has been designed and constructed. The performance of the detector has been studied in a test beam at CERN. Results are presented on the hit efficiency and the position resolution as a function of position along the strips. With a hit efficiency of 99.5 % and a spatial resolution of typically 35 μm the performance of these detectors exceeds that of other candidate technologies for the precision forward tracker of the ATLAS inner detector.

Introduction

The ATLAS technical proposal contains a description of the inner detector comprising a precision tracker at lower radii supplemented by an straw-tube system at outer radii [1]. It is proposed that the central region of the precision tracker be instrumented with silicon microstrip detectors whilst the forward regions are covered by either microstrip gas chambers (MSGCs) or silicon microstrip detectors. In either case gallium arsenide (GaAs) detectors are placed at the smallest radii were the radiation levels are largest. Following the submission of the technical proposal the design of the inner detector has continued to evolve and, in particular, the ATLAS inner detector community has recently decided to replace the MSGCs in the forward region with fan geometry silicon detectors giving an integrated semiconductor tracker. As input to this decision, a prototype 12 cm long fan-geometry silicon detector, having the same spatial resolution capability as an MSGC, i.e ~ 35 μm, was developed. This paper deals with the design, construction and test beam evaluation of this detector when coupled to LHC speed front-end electronics.

Detector Geometry

Figure 1 shows a quarter section view of the current layout of the integrated semiconductor tracker. The barrel section consists of 4 stereo layers with radii between 300 mm and 520 mm and length ~ 760 mm. The forward regions each consist of 9 discs supporting silicon detectors covering a radial extent of 320 mm to 560 mm except for those at large z where the coverage is limited to $|\eta| = 2.5$. Several of the wheels at smaller z are extended to lower radius using GaAs detectors giving 5 space points per track out to $|\eta| = 2.5$. Each layer consists of a ϕ-u or ϕ-v configuration with 40 mrad. stereo angle. The disks are divided into two rings of radial extent 12 cm or 6 cm depending on the location. There are 50 modules in an outer ring and 40 in the inner. The requirements of the second level trigger necessitates a design in which the $R\phi$ coordinate is measured directly by means of radial readout strips. The performance specifications have been unified over the whole η range giving a position resolution requirement of $\sigma_{R\phi} = 15$ μm and σ_z or $\sigma_R = 770$ μm per measurement point. This can be realised with detectors (capacitive or direct coupled) with binary readout at 75 μm pitch or capacitively coupled detectors with an intermediate strip and analogue (direct or digitised) readout at a pitch of 112.5 μm.

Design of a Fan Geometry Silicon Prototype

A simple DC detector (*p*-strip in *n*-type bulk) suitable for high voltage operation was designed at Liverpool and manufactured by Micron Semiconductor Limited [2]. To reduce cost a full length half width detector was designed. The 12 cm long module contained 256 strips with strip pitches varying from 103.1 μm to 144.9 μm giving a active width of 3.71 cm at the broad end and 2.64 cm at the narrow end. The module was fabricated from two separate detectors, each approximately 6 cm in length, obtained from a single 4" diameter wafer as shown in figure 2. This design was chosen to give a similar spatial resolution performance to that of the MSGCs in the ATLAS MSGC tracker, i.e ~ 30 to 40 μm.

A section of one of the mask designs is shown in figure 3 illustrating the readout strips and their bond pads, the guard rings and the scribe lines defining the edge of the wafer. Following a study of the high-voltage capability of different guard ring structures, undertaken by Micron Semiconductor Limited, a simple guard ring structure consisting of 3 continuous *p*-strips surrounding each detector was adopted. The aim of the guard rings is to reduce the leakage current in the guard region when high depletion voltages are required due to radiation damage. This is accomplished by limiting the extent of the depletion region such that areas near the edges of the detector, where the lattice has suffered damage due to mechanical processing, remain undepleted even when high bias voltages are applied.

In designing a detector with a variable pitch the choice is whether to vary the width of the *p*-implant, or the width of the gap between implants or both. The need to maintain a constant charge collection efficiency over the length of the detector provides an argument for maintaining a constant gap between the readout strips. A second design consideration is the necessity of minimising the inter-strip capacitance in order to reduce the series noise in the electronics. Given the variation of strip pitch required the following compromise was adopted. For the inner wafer the gap between strips was a constant 68 µm so that the width of the *p*-implant varied from 35 µm to 56 µm. In the case of the outer wafer the gap was kept constant at 80 µm and the implant width varied from 44 µm to 65 µm.

Wafer Characterisation

The leakage currents and inter-strip capacitances of the wafers were measured using a probe station with a source measure unit and a capacitance-voltage analyser running under the control of a PC running LabView [3]. An example of the inter-strip capacitance measurements is shown in figure 4. The inter-strip capacitance after full depletion was typically about 5 pF for a 6 cm long detector. The capacitive load, represented by two such detectors daisy-chained together, is therefore well within the 15 pF specification coming from the noise requirements of the front-end electronics.

The leakage currents were measured as a function of the depletion voltage. An example of the variation of leakage current with depletion voltage is shown in figure 5 for a strip in the centre of a wafer. The leakage current increases slowly with voltage until breakdown occurs at a voltage of ~ 290 V. Breakdown tended to occur at lower voltages when the strip tested was close to the edge of the wafer.

Module Construction

The prototype detector was constructed to be read out using an APV5 front end chip [4]. The two wafers were glued onto a carbon fibre support frame and then wire bonded together. A hybrid equipped with an APV5 chip was connected to the detector by means of a fan-in. The necessary control logic was included on a separate board and read out via optical fibres into VME-based SIROCCO ADCs [5]. The arrangement is shown in figure 6. The detector was mounted in a light tight box with thin windows of aluminized mylar to minimise multiple scattering.

Test Beam Studies

The detector was evaluated in the H8 test beam at CERN as part of the programme of the ATLAS Inner Detector Group. The test bed consists of a precision granite block on which various detectors are mounted [6]. A telescope consisting of 6 planes of silicon strips mounted in 3 pairs define the beam direction and test modules are mounted on additional supports. The main aims of the tests were to measure the efficiency and the spatial resolution as a function of the position along a strip.

The detector under test was mounted on a support stand allowing up to 12 positions along the length to be illuminated by a charged particle beam of cross-section 1 cm (horizontal) by 2 cm (vertical) at normal incidence. The location of the beam on the test detector was measured relative to the wafer break giving a full range of - 6 cm (narrow end) to + 6 cm (wide end). The silicon telescope was used to predict hit positions to an accuracy of ~2 µm [7]. Due to the wide strip pitch and the lack of any charge sharing mechanism, the number of two-strip clusters was expected to be low giving a spatial resolution of strip pitch $/\sqrt{12}$, i.e ~ 35 µm at the mid point of the detector.

Data processing

Before the final analysis was performed all the necessary ADC pedestal levels and electronic noise parameters for the test detector were computed and saved to disk. This was made complicated by the pipe-lined nature of the APV5 readout chip. In addition to the conventional common mode and channel-to-channel pedestal variations, the pedestals also depended on the pipe-line location. This necessitated the construction of a two-dimensional pedestal map to produce the best possible signal/noise ratios.

Pulse height and efficiency variation

Particle tracks, reconstructed from the hits in the beam telescope, were used to define an expected hit position on the face of the prototype module. The channel number of the nearest strip was computed using a set of pre-determined alignment constants. The corresponding signal was defined as the pulse height in ADC counts divided by the RMS of the electronic noise distribution of the predicted channel.

Figure 7 shows a histogram of the pulse height spectrum, expressed in units of signal/noise at four different locations along the length of the strips. These spectra follow the usual 'Landau'-type form and show no sign of any position dependence. The most-probable pulse height corresponds to a signal/noise ratio of ~ 11/1.

The detection efficiency and fake hit rate were studied as a function of position along the strips using the pulse-height on the expected strip to define a hit. Figure 8 shows the variation of the hit efficiency as a function of the pulse-height threshold applied, in units of signal/noise, for the four locations along the strips. The efficiency is greater than 95 % for a threshold less than $7\sigma_{noise}$ and is ~ 99.5 % at a $4\sigma_{noise}$ cut as shown in the inset. There is no significant variation of the efficiency with position along the detector length.

The fake hit rate is measured by using the same sample of tracks used in the efficiency determination. Using the beam telescope data the channel number of the expected strip is identified. This strip and its five nearest neighbours on each side are masked out and the hit finding algorithm is applied to the remainder of the test detector. The fake hit rate is defined as the number of times any strip exceeds the threshold normalized to the number of strips in the detector and the number of events in the sample. Figure 9 shows the fake hit rate, at one beam location as a function of the pulse-height threshold applied. The data show a rapid decrease at small thresholds due to the electronic noise, followed by a more gradual decline at larger thresholds. At a $4\sigma_{noise}$ threshold the fake hit probability is 2.10^{-4} and compares well with the requirement of being less than 10^{-3}.

Resolution studies

Hits were found in the test detector independently of the data from the beam telescope. A hit was defined if a strip had a significance greater than $3\sigma_{noise}$ and, when combined with the larger of its two neighbours, the cluster had a total pulse-height greater than $4\sigma_{noise}$. A hit residual was formed from the expected location derived from the beam telescope and the observed hit location as determined by the above algorithm. Figure 10 shows the distribution of hit residuals for all clusters, for data taken near the narrow end of the detector, after the alignment with the beam telescope had been performed. The fraction of two strip clusters, indicated by the shaded part of the histogram, was found to be 13 % and is a result of the lack of a charge-sharing mechanism in this wide-pitch geometry detector. The spatial resolution, given by the RMS of the residual distribution, is ~ 30 μm. The contribution to this from the telescope extrapolation error of 2 μm is negligible and has been ignored.

Figure 11 summarises the data on the variation of the spatial resolution as a function of the beam position along the strips. In the upper part of the figure the measured RMS is plotted with reference to the right hand scale as a function of the beam position. In the lower part the fractional RMS, i.e RMS/pitch is plotted with reference to the left hand scale. Also shown are lines corresponding to pitch/$\sqrt{12}$ and $1/\sqrt{12}$ for comparison. In general, the spatial resolution is slightly better than pitch/$\sqrt{12}$ and the fractional resolution is approximately constant. There is a hint that at the narrowest pitch, i.e. ~ 100 μm the fractional resolution improves further due to the increased occurrence of double-strip clusters.

Conclusions

A prototype fan-geometry silicon detector module matching the performance specifications of the MSGC option for the forward precision tracker in the ATLAS inner detector has been designed and constructed. The performance characteristics of this detector have been investigated in a test beam at CERN. The hit detection efficiency was found to be > 99.5% at $4\sigma_{noise}$ threshold and independent of the beam position along the length of the strips and the spatial resolution was found to be consistent with pitch/$\sqrt{12}$ as expected. Following the decision by ATLAS to pursue the silicon option for the forward region precision tracker a common silicon technology for both the barrel and forward regions that meets the improved performance specifications is being developed.

Acknowledgements

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References

[1] ATLAS Technical Proposal CERN/LHCC/94-43.

[2] MICRON Semiconductor Limited, Lancing, UK.

[3] Trademark of National Instruments Inc.

[4] Radiation hard 128-channel silicon readout chip fabricated by Harris (USA). CERN/DRDC 94-39. RD20 Status report.

[5] SIROCCO - VME based MUX-ADC from Strasbourg.

[6] Liverpool / CERN silicon telescope constructed in 1994 for ATLAS.

[7] P. P. Allport "ATLAS Test Beam Results". These proceedings.

List of Figures

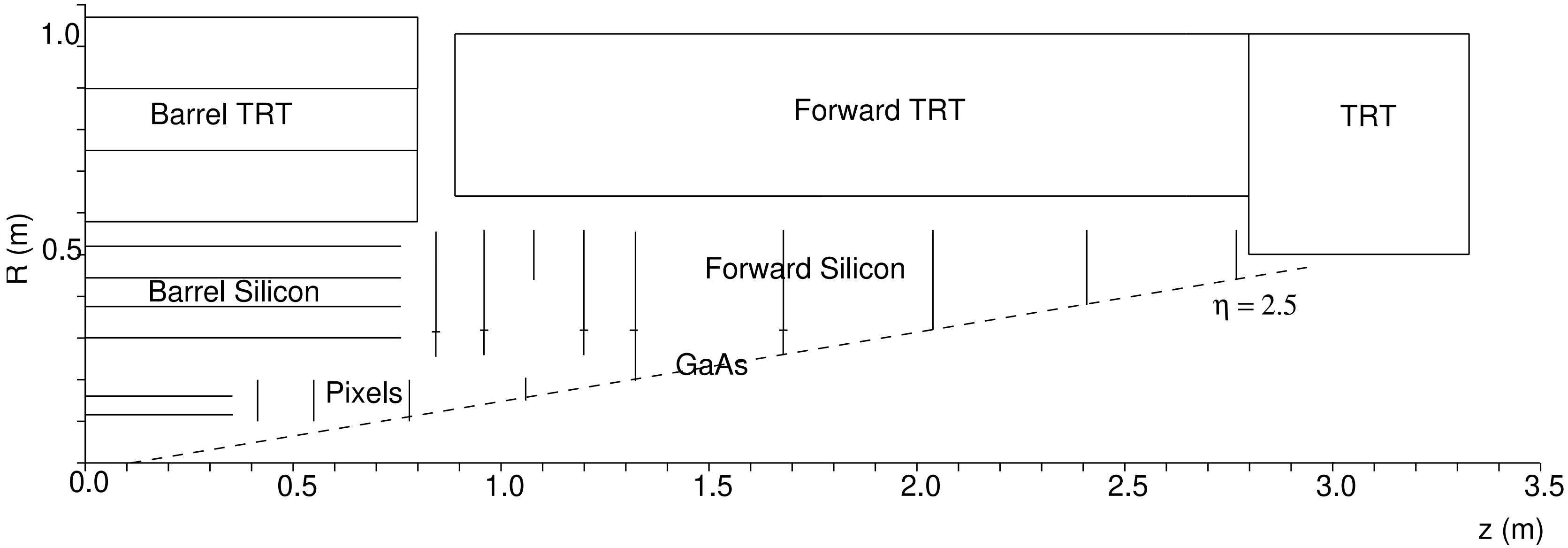

Barrel TRT
Forward TRT
TRT
Barrel Silicon
Forward Silicon
GaAs
Pixels
$\eta = 2.5$
R (m)
z (m)
1.0
0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

Figure 1

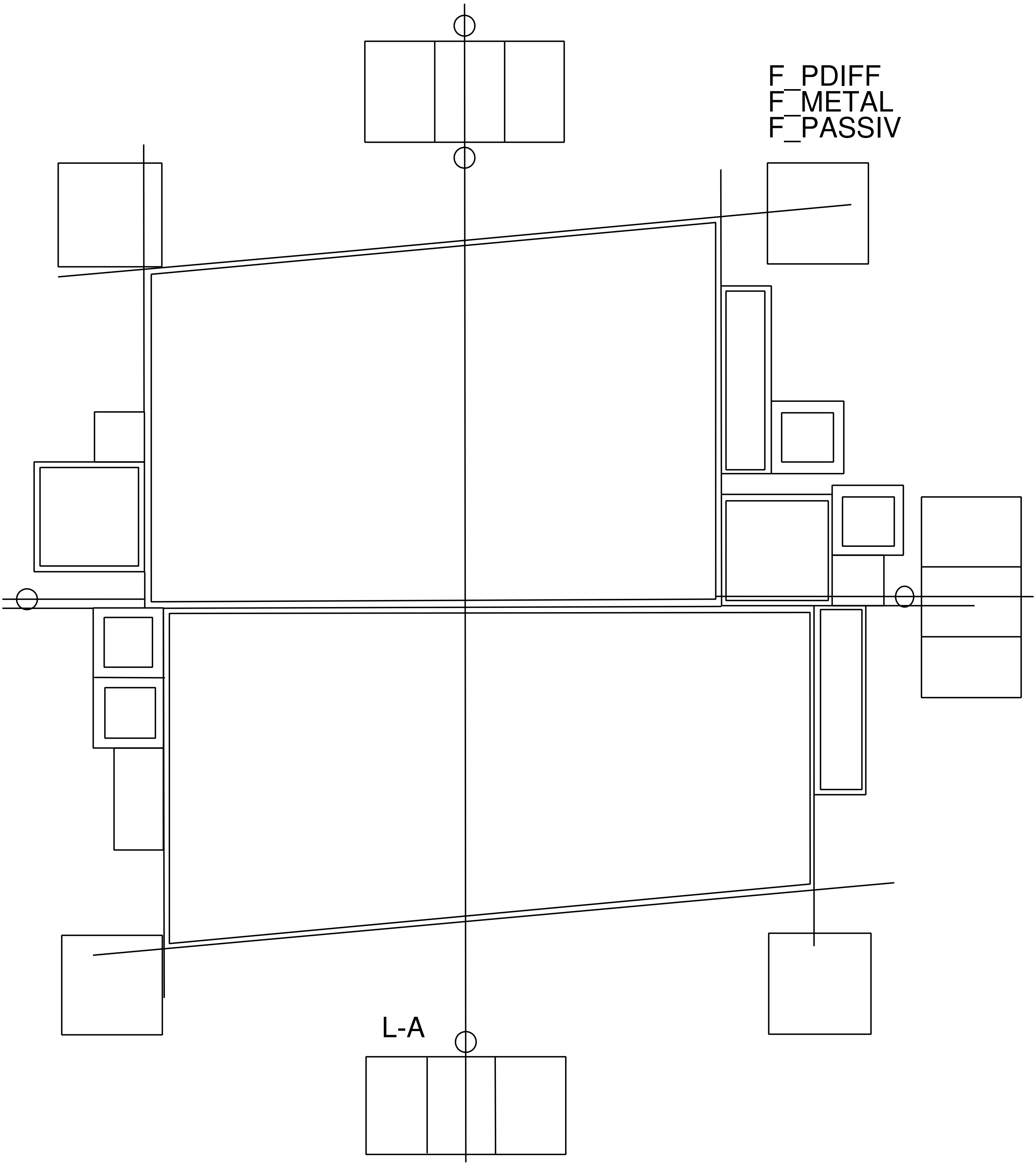


Figure 2

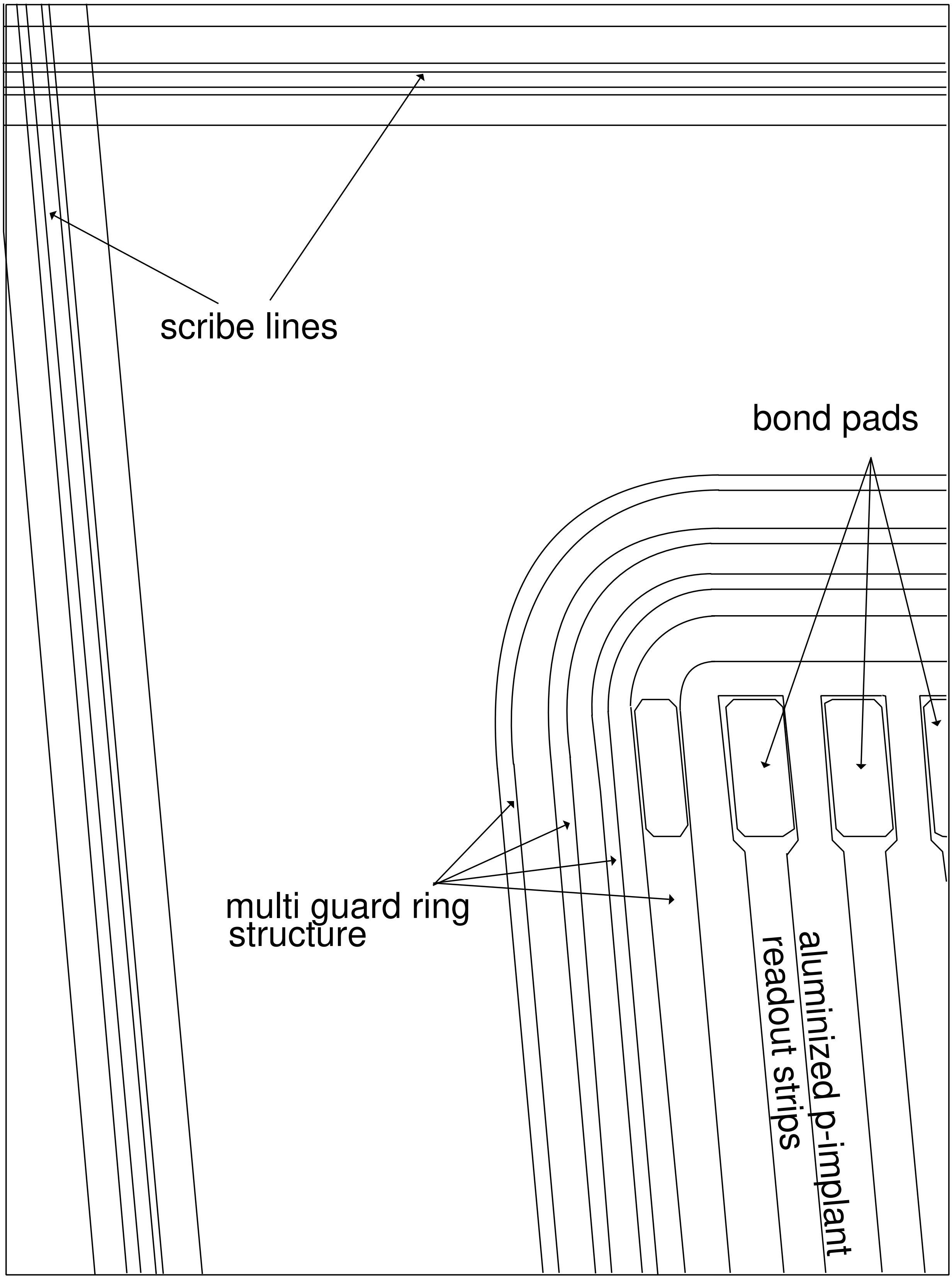
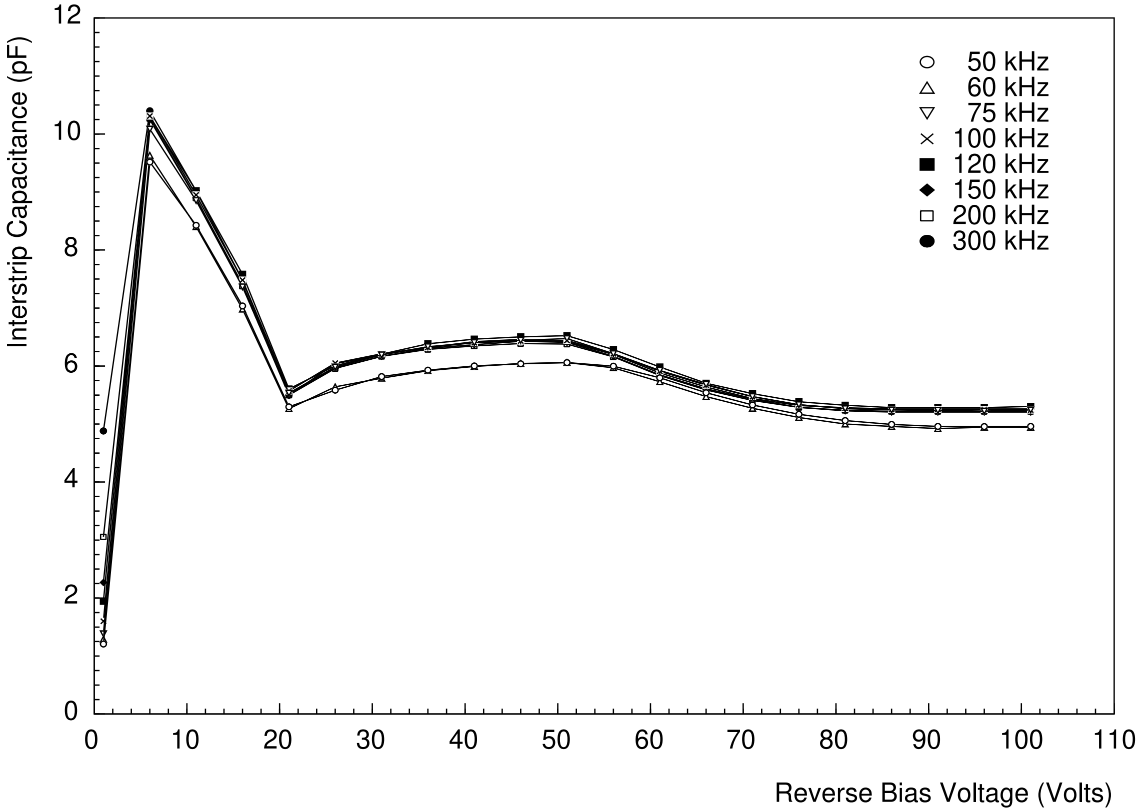

scribe lines
bond pads
multi guard ring
structure
aluminized p-implant
readout strips

Figure 3



Interstrip Capacitance (pF)
Reverse Bias Voltage (Volts)
50 kHz
60 kHz
75 kHz
100 kHz
120 kHz
150 kHz
200 kHz
300 kHz
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
80
90
100
110

Figure 4

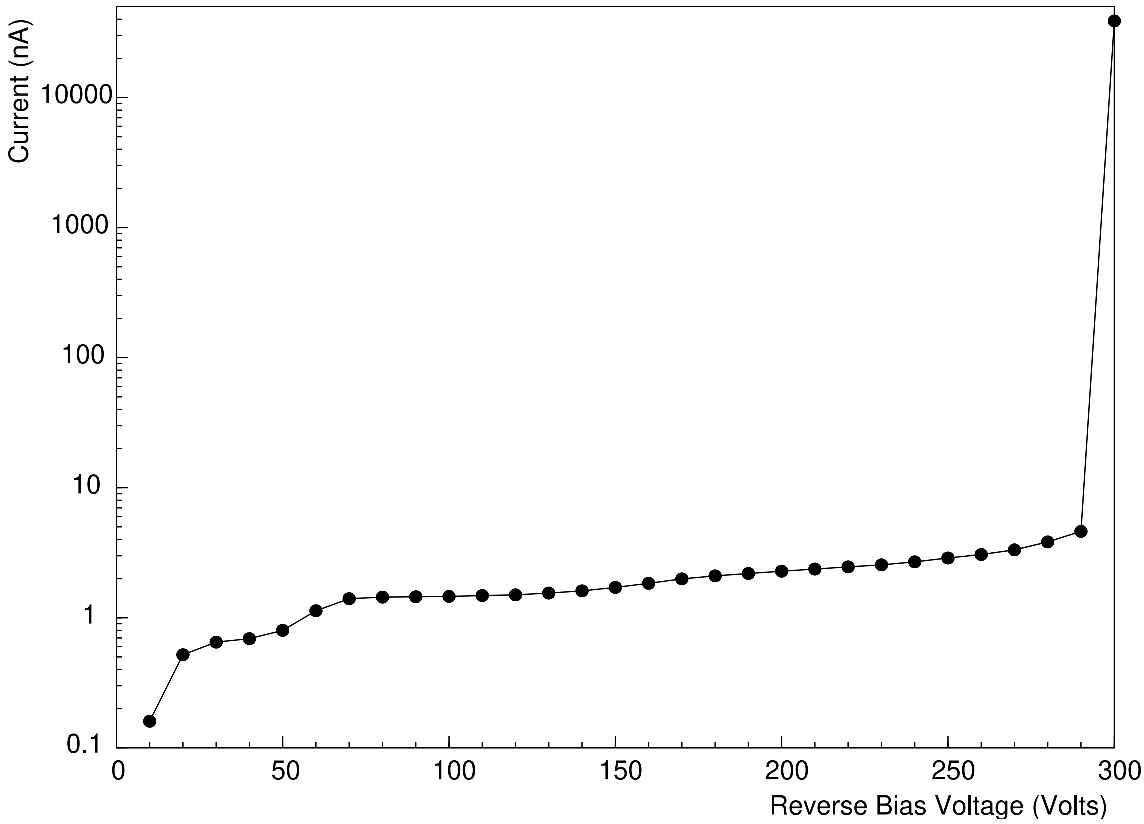

Current (nA)
10000
1000
100
10
1
0.1
0
50
100
150
200
250
300
Reverse Bias Voltage (Volts)

Figure 5

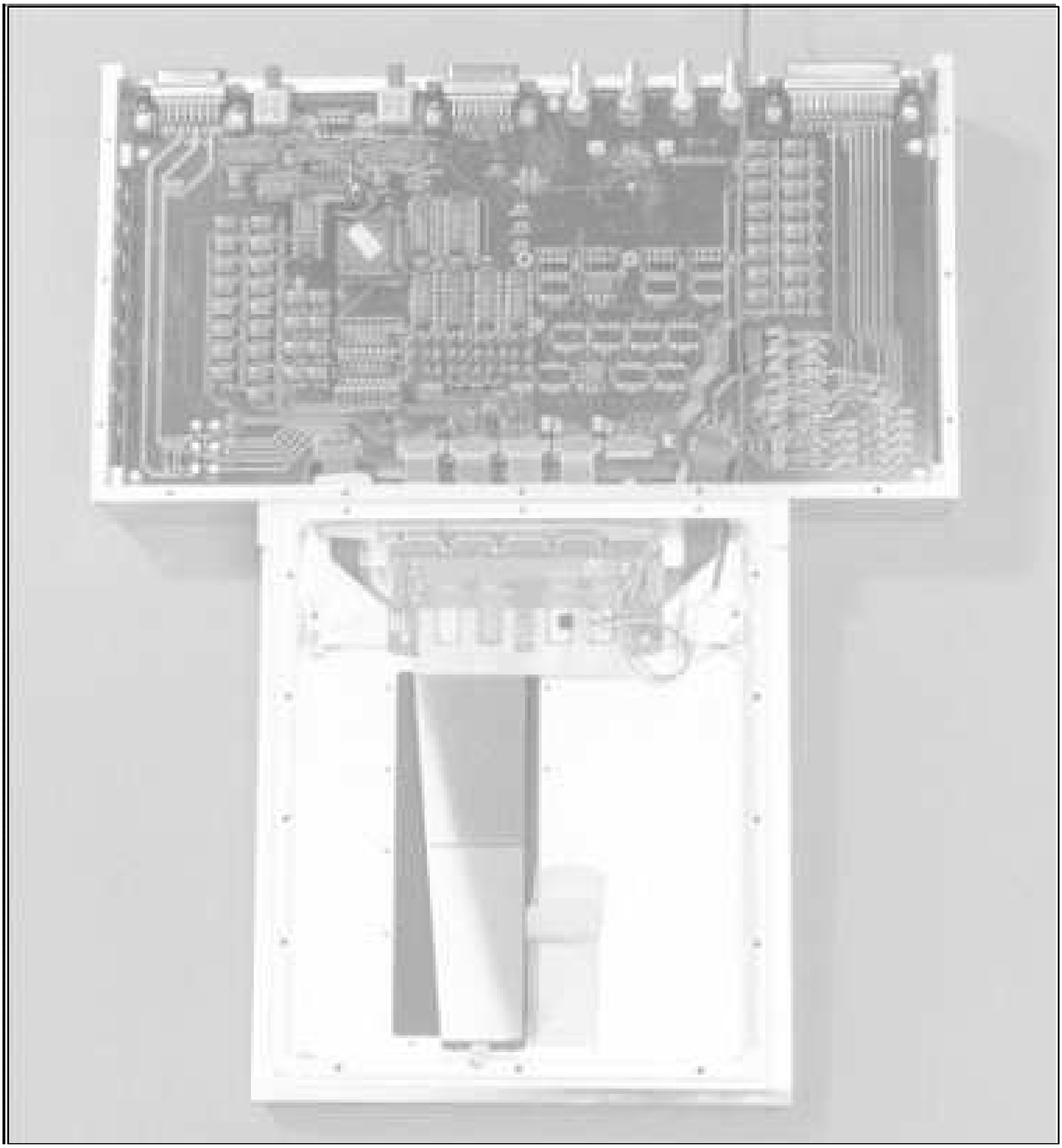
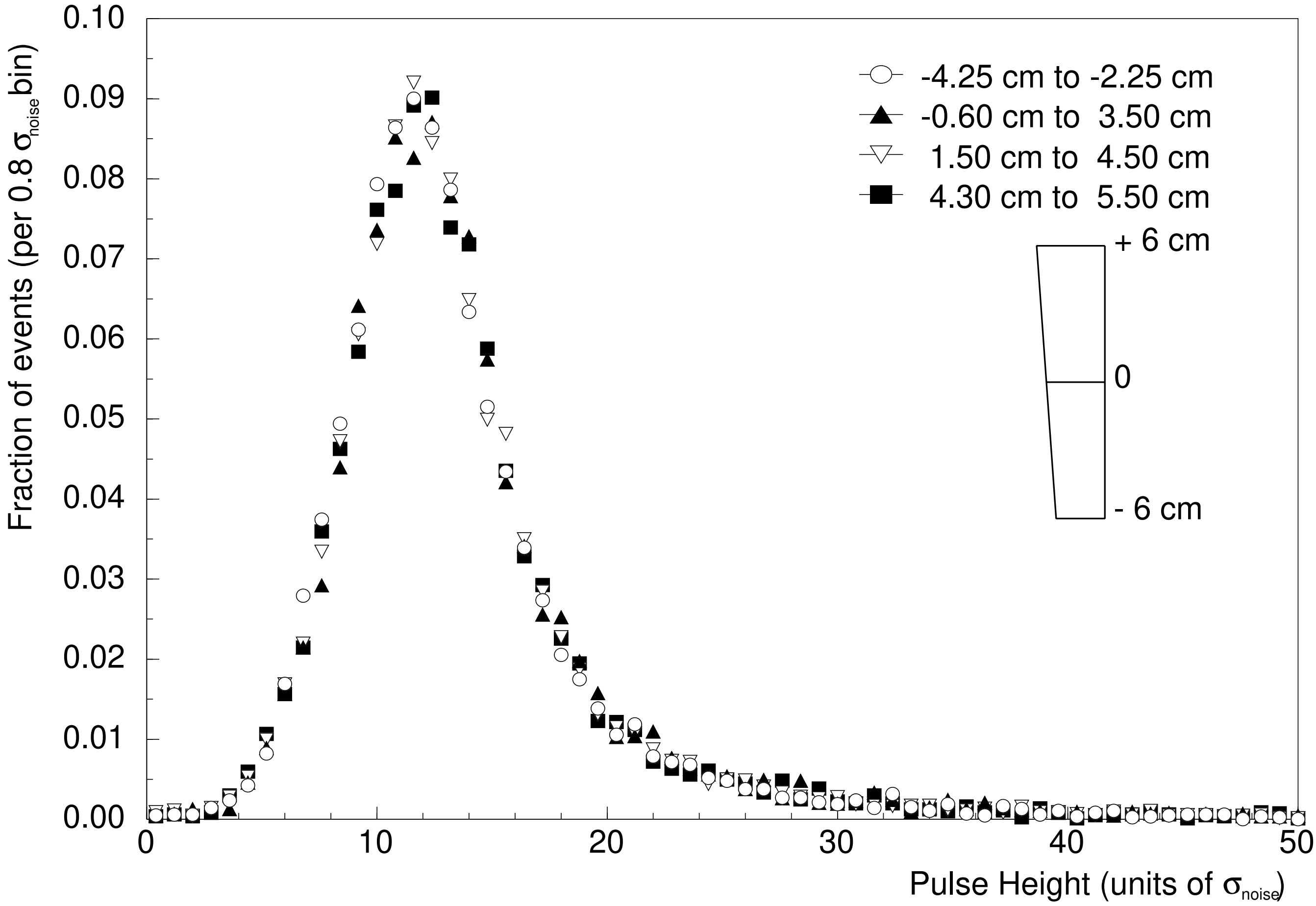


Figure 6



0.10
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0.00
Fraction of events (per 0.8 σnoise bin)
0
10
20
30
40
50
Pulse Height (units of σnoise)
-4.25 cm to -2.25 cm
-0.60 cm to 3.50 cm
1.50 cm to 4.50 cm
4.30 cm to 5.50 cm
+ 6 cm
0
- 6 cm

Figure 7

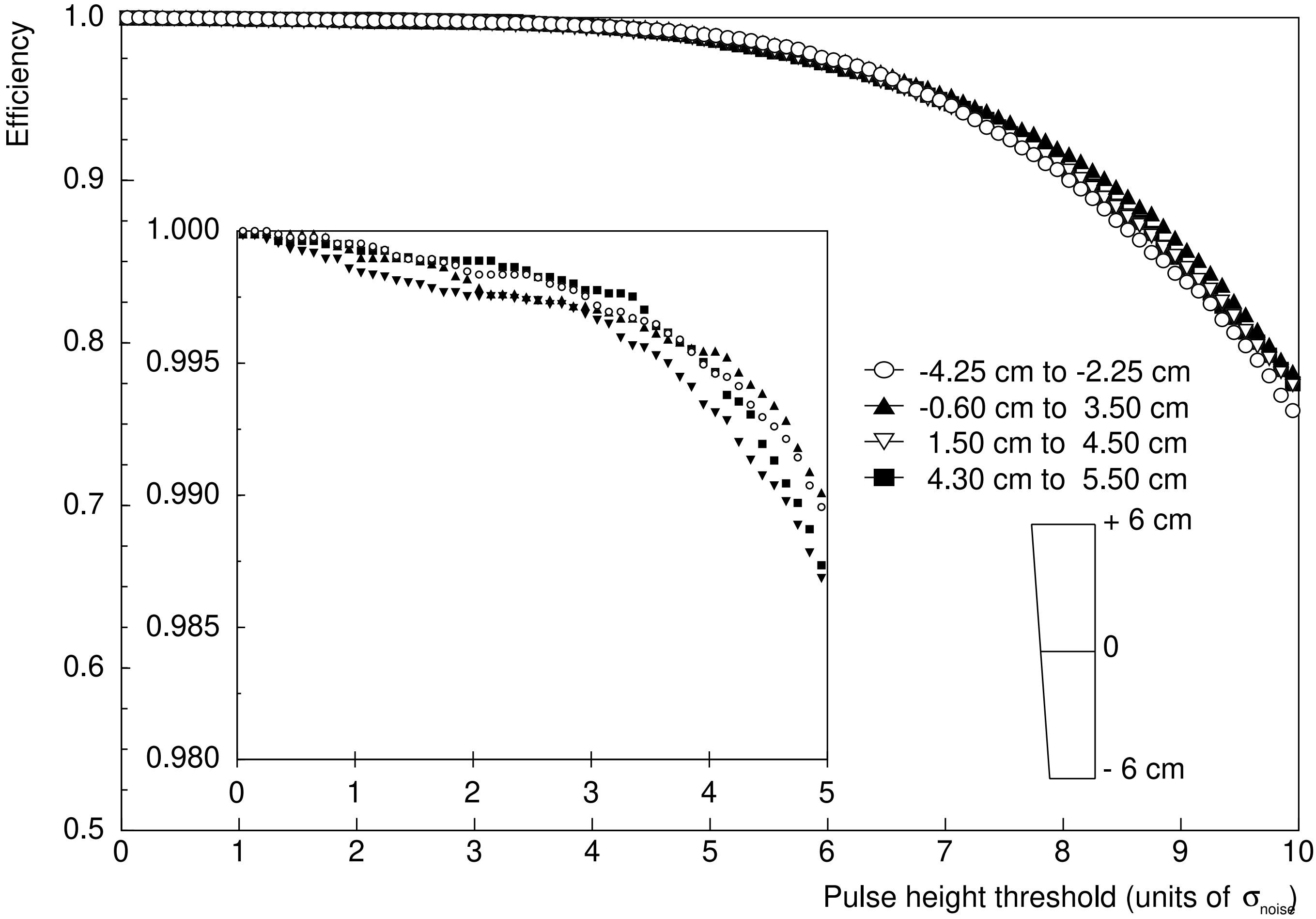

Efficiency
1.0
0.9
0.8
0.7
0.6
0.5
0
1
2
3
4
5
6
7
8
9
10
Pulse height threshold (units of σnoise)
1.000
0.995
0.990
0.985
0.980
-4.25 cm to -2.25 cm
-0.60 cm to 3.50 cm
1.50 cm to 4.50 cm
4.30 cm to 5.50 cm
+ 6 cm
0
- 6 cm

Figure 8

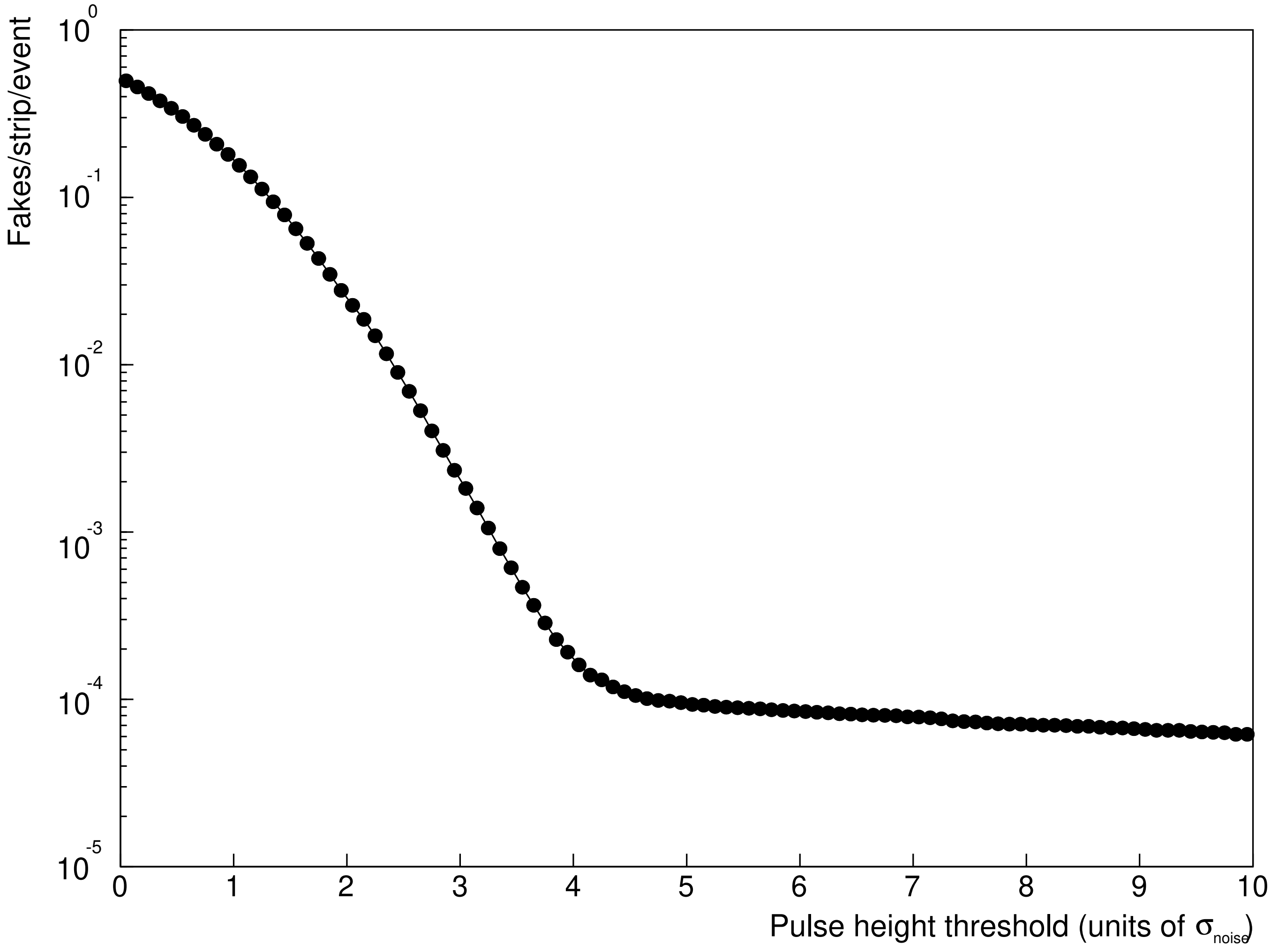

Fakes/strip/event
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
0 1 2 3 4 5 6 7 8 9 10
Pulse height threshold (units of σ_{noise})

Figure 9

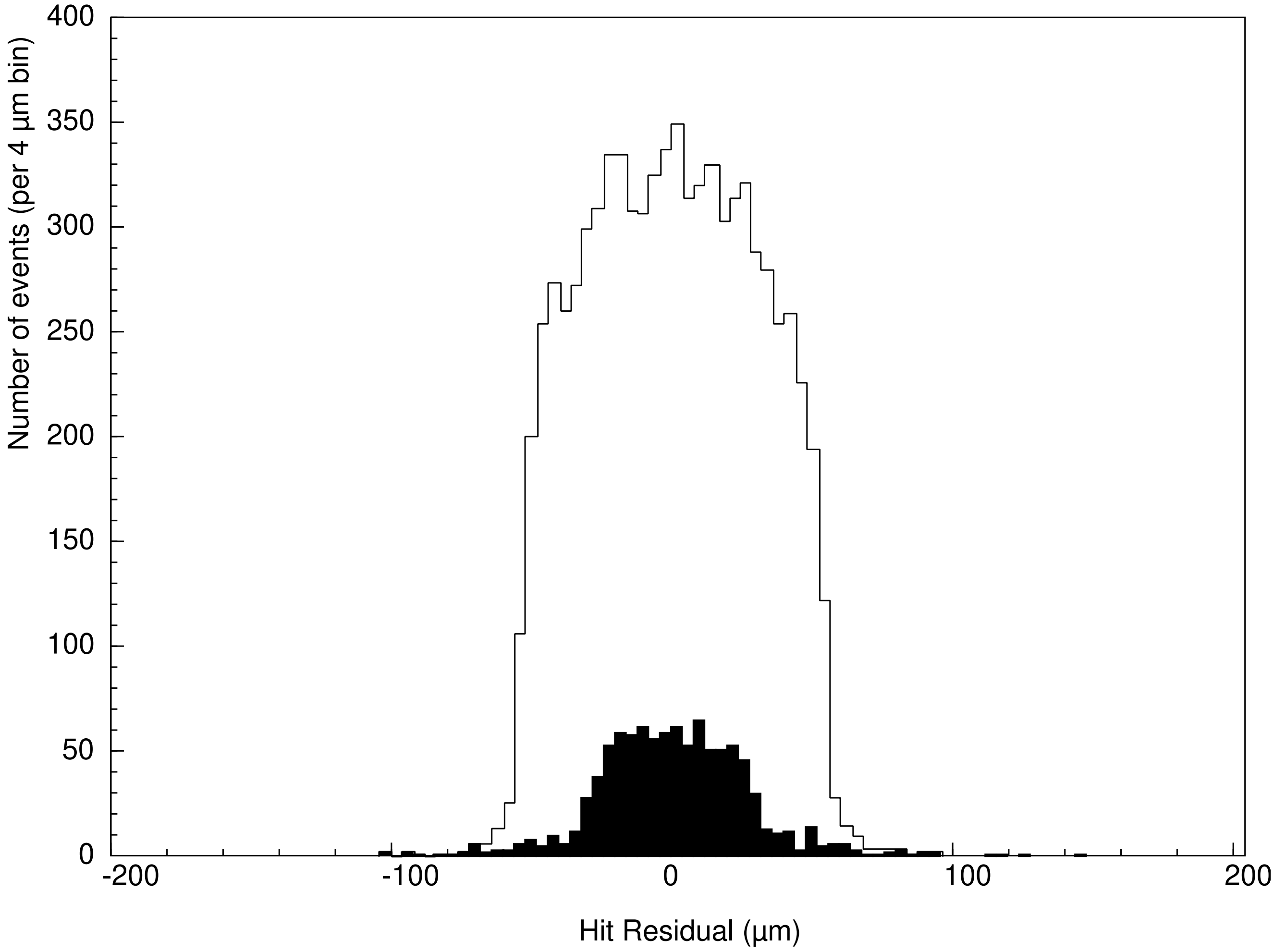

400
350
300
250
200
150
100
50
0
Number of events (per 4 µm bin)
-200
-100
0
100
200
Hit Residual (µm)

Figure 10

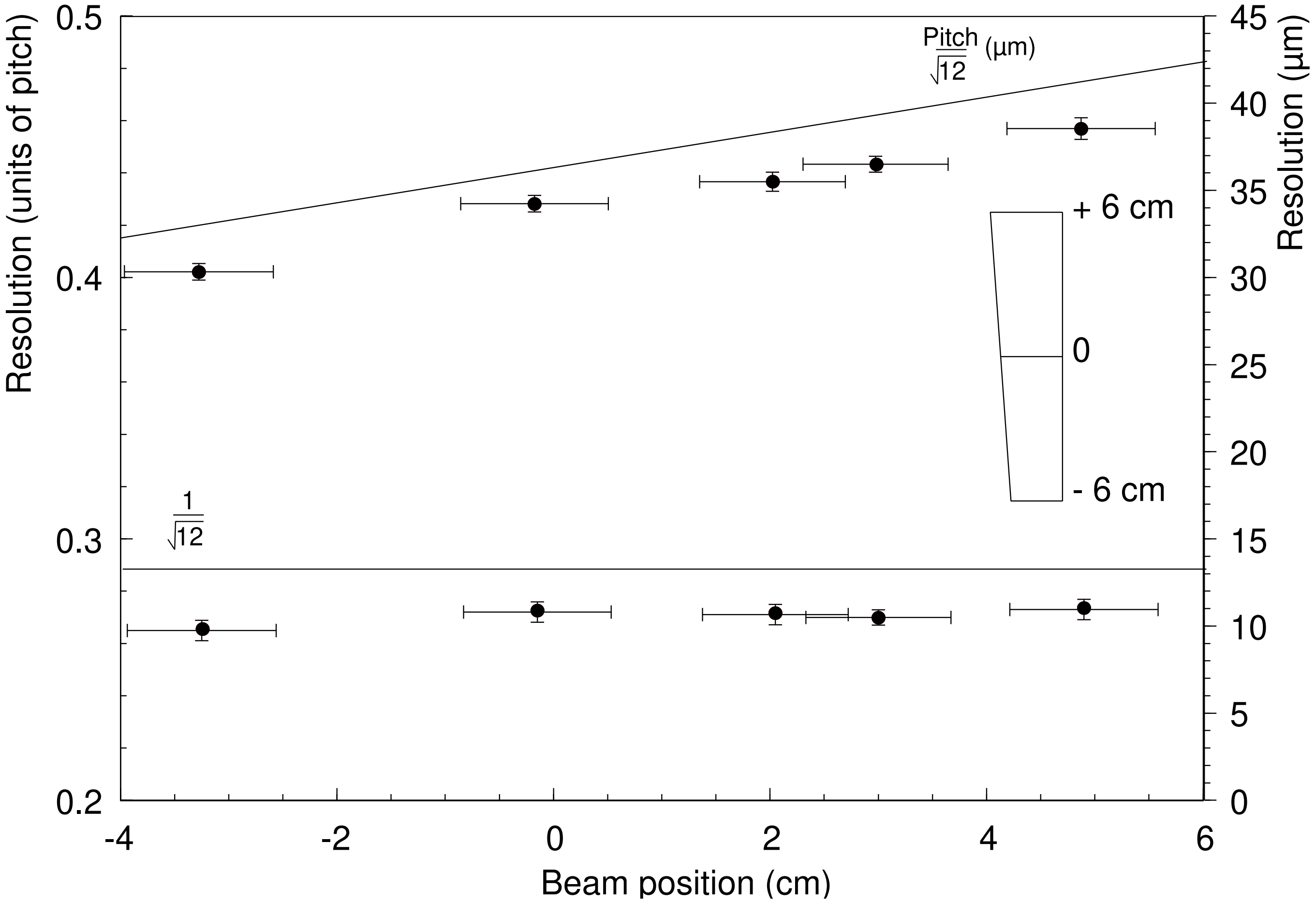

Resolution (units of pitch)
Resolution (µm)
Beam position (cm)
Pitch/√12 (µm)
1/√12
+ 6 cm
0
- 6 cm
0.5
0.4
0.3
0.2
45
40
35
30
25
20
15
10
5
0
-4
-2
0
2
4
6

Figure 11

the end of this παπερ