ATLAS BEAM TEST RESULTS

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Many different configurations of electronics and semiconductor strip detectors were studied in 1995 using the ATLAS tracking detector test area at the H8 beam-line of the CERN SPS. A significant fraction of these investigations are presented elsewhere in this volume and this paper will concentrate on the results concerning silicon strip detectors read out with electronics preserving the pulse height information. Data have been collected with the ADAM, APV5 and FElix read-out chips on a number of different detectors. The first results are presented for read out with LHC electronics of detectors to the ATLAS-A specification of 112.5μm pitch, employing $n-$strips in $n-$type silicon, capacitive coupling and intermediate strips. It is demonstrated that with adequate signal/noise, a spatial resolution of $\simeq$13μm is attainable with these detectors.

1 Introduction

Semiconductor micro-strip detectors provide a vital component for the tracking over the whole acceptance range ($\mid \eta \mid < 2.5$) of the ATLAS Inner Detector[1].

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[1] SINTEF/SI, Oslo, Norway

Extensive R&D has been required to show the viability of 128 channel front-end read-out chips, fast enough to operate at the 40MHz beam crossing rate at the LHC whilst dissipating $\lesssim$4mW of total power per channel. For high tracking efficiency, noise values of $\leq$1500 ENC are required at the capacitive load represented by a 12cm length silicon strip detector. Results using electronics with a fast shaper and discriminator implemented in bipolar technology, followed by a CMOS *binary* pipeline (allowing for the $\sim 2.5\mu$s Level 1 trigger latency) are presented elsewhere in this volume[2,3]. In this article, results with architectures using CMOS front-end amplifiers followed by *analogue* pipelines are presented.

There are two categories of such electronics under consideration within ATLAS. With *digital* electronics, the signal is digitised and the data sparsified by the front-end electronics at the detector giving encoded pulse height and channel number information for strips above a pre-set threshold. This is transmitted digitally to the control room[4]. In the case of *analogue* electronics all the amplifier output levels for the trigger time slot are time-multiplexed off the detector as an analogue signal to be digitised and sparsified remotely[5]. A further difference in the architectures presented here is that the digital electronics (ADAM) uses a fast CMOS front-end amplifier before the analogue pipeline, effectively giving all the pulse-height information in a single 25ns time-bin. The current implementations of the analogue scheme (FElix-128, APV5) use a slow shaper ($t_{\mathrm{peak}} \sim$ 75ns) of well defined response function and the signal in the correct time-slot is recovered using a weighted summing technique, effectively performing a deconvolution, implemented for each channel of the chip prior to read-out. (See [6] for details on the ATLAS read-out chips.)

Whilst an understanding of the electronics performance was a major concern for the test-beam programme during 1995, development of full-sized ATLAS modules incorporating the prototype electronics and detectors was also undertaken. Although these modules were shown to work well functionally, not all the final performance specifications were met by the read-out chips employed. Additional studies were undertaken which allowed specific detector designs (fan geometry and $n-$strip in $n-$type) to be further investigated. The former were prototypes for forward tracking[7], whilst the latter were designed to one of the agreed specifications for the ATLAS silicon strip detectors[1]. Preliminary results on these ‘ATLAS-A’ specification detectors, using improved LHC electronics, were obtained at the end of the test-beam period. These show very encouraging results for this detector design, which employs intermediate strips and charge division on a single-sided $n-$side read-out.

2 The H8 Test Beam

In 1994 a hodoscope consisting of up to 4 cross-planes of 50μm pitch 3.2×3.2cm strip detectors with read-out via the CERN-Oslo 'Viking' chip[8] was commissioned in the H8 area. The signal/noise for these modules was ~75 implying very high efficiency track reconstruction. However the peaking time of these chips is $\sim 1\mu$s; much longer than that required of the LHC electronics. Precision mechanics supplied by Liverpool allowed the detectors to be mounted onto locating fixtures on an 80cm long solid granite baseplate, giving a placement reproducibility of $\sim$1μm. This system has been measured in the 1994 and 1995 beam tests to provide an extrapolation precision at the test detectors of $\leq 2\mu$m.

Read-out of this telescope is performed using LEP VME modules (Sirocco's), with chip control via a Viking sequencer box. The same read-out modules were used for the time-multiplexed outputs of the prototype analogue LHC electronics but the clocking of the analogue pipelines, the trigger inputs and the timing of the output sampling required a more sophisticated fully programmable fast sequencer, which was designed and supplied by the Rutherford Appleton Laboratory (RAL). The DAQ was built around commercial VME units and was designed and implemented by the Cambridge, CERN, and Oslo groups with monitoring and online tape logging implemented by the Melbourne group.

A separate system for the digitised read-out scheme was provided by groups from Bern, CERN, Geneva and Melbourne. The system implements a complete digital read-out scheme for ATLAS modules with front-end and signal processing chips, a read-out controller, an optical link, and high rate acquisition and control VME boards[9]. The system operated successfully at LHC clock speeds, and largely according to LHC performance specifications. Studies with binary electronics were also integrated into the overall scheme using a common protocol and with VME based read-out hardware provided by the Lawrence Berkeley Laboratory (LBL), UC Irvine, UC Santa Cruz and Oxford groups[3].

Data from all these systems, along with that from several runs with gallium-arsenide detectors were monitored on-line and logged to tape. Offline monitoring was performed using code coordinated by the RAL group.

3 The Digital Electronics Results

300μm thick detectors of 200μm pitch and 6cm length were designed to the RD2 specification[4] and fabricated by Hamamatsu. These were tested with a

32 channel version of the ADAM architecture[4,10]. The ADAM chip, which is currently the only digital front-end working at LHC speed, has a fast low power CMOS amplifier, NICON[11], giving a 42mV signal for an injected charge of 25000 electrons. This is followed by a 2μs double-correlated analogue pipeline and a multiplexer, prior to digitisation by a pipelined ADC. As noted, the ADAM chip was implemented with a full LED-based optical read-out system. For the full system, a signal/noise of $\sim$ 11 (figure 1) was achieved[6], giving $> 99\%$ efficiency at a cut of four times the noise and also demonstrating the expected spatial resolution. Since the signal/noise is dominated by the intrinsic pre-amplifier noise (and not subsequent stages in the chip), further development foresees the use of the same architecture but using a bipolar pre-amplifier. This should improve the signal/noise but at a small, although acceptable, increase in power dissipation. This configuration is intended for radiation damage studies to read out irradiated detectors at full LHC speed. The AROW chip development[6], uses the bipolar front-end amplifier and an integrated Wilkinson ADC on a full 128 channel chip, building on the experience gained in the ADAM studies.

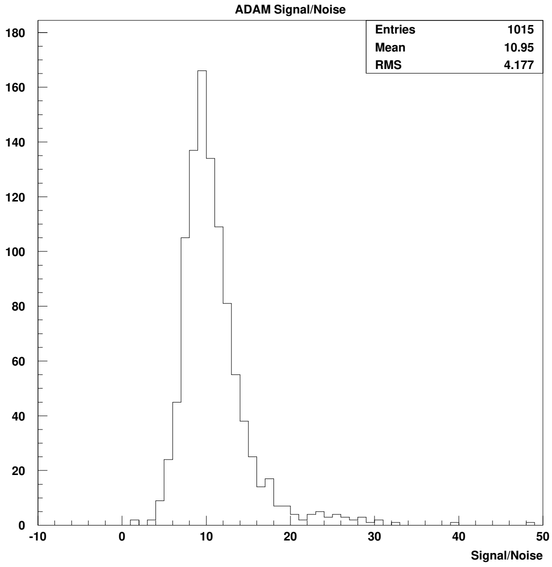


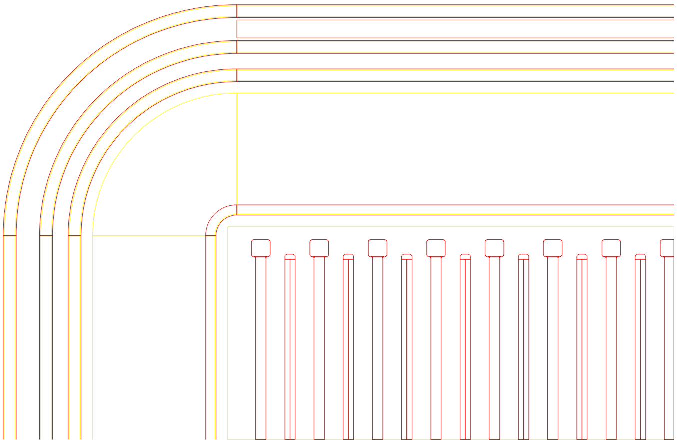
Fig. 1. *Pulse height distribution, in units of the single channel noise, for a 200μm pitch, 300μm thick Hamamatsu detector read out with the ADAM electronics.*

4 The ATLAS Prototype Detector Designs

The binary electronics[3] was used with detector designs where all diode strips are read out. This leads to high efficiency with an anticipated resolution of approximately pitch/$\sqrt{12}$. There may also be scope to use this electronics with charge division detector designs, which with 50% single hit clusters and 50% doubles should approximate more to a resolution of pitch/$\sqrt{48}$. Whilst this latter scheme deserves further investigation, the read out of every strip provides a robust and rather straightforward technological solution which is a strong contender for the final ATLAS design.

In the case where analogue information is available, the ratios of pulse heights on adjacent strips can be used to interpolate giving the coordinate of the track position to a much better resolution than pitch/$\sqrt{12}$. The only concern with this approach (which is widely used at LEP and in many fixed target experiments) is that if the signal/noise is marginal, the efficiency of the detector can be compromised[12].

ATLAS is investigating detector designs based on n^+-type strips because after radiation damage the lightly doped $n-$type bulk inverts to $p-$type with an effective p doping that increases with dose. This leads to high values of the voltage needed to fully deplete the detector. Whilst double-sided detectors are being actively pursued within ATLAS, these do suffer from the disadvantage that for the $p-$strip side to be effective, full depletion after irradiation plus some over-depletion is required. The $n-$strips, however, remain acceptably efficient at lower voltages, with the effect of under-depletion being the fall off in the sensitive volume[2] (which is only expected to fall as $\sqrt{V_{\text{BIAS}}}$).



voltages were ~20V. The isolation p^+ implant is also 20μm wide with an implant dose of $\sim 2 \times 10^{13}/\mathrm{cm}^2$ through a thin oxide. There is one intermediate strip to linearise charge division and the read-out pitch is 112.5μm. The devices incorporate three guard-rings to promote higher voltage operation. The $p-$side of the device also requires photolithographic processing to give a diode implant which matches the sensitive area of the $n-$side with guard-rings also mirroring the $n-$side. The devices are 6×6cm in size, cut from a 4" wafer of high purity $< 111 >$ silicon, giving 512 read-out strips per detector. The masks were designed at Liverpool in collaboration with Cambridge, QMW London and RAL, and they were fabricated by CMF at RAL. The detectors were fabricated by Micron Semiconductor (UK) Ltd.

5 The APV5 Module Results

Pairs of these detectors were assembled into prototype ATLAS *z-modules*[13]. In this scheme, modules are produced with pairs of 6cm detectors daisy-chained together and subsequently mounted with another 40mrad stereo pair onto a module. The electronics sits to the side of the detectors next to the cooling structures. One possibility with this design is to mount the modules onto beryllium staves which run the length of the barrel and which provide the services, read-out and cooling all integrated onto one mechanical support structure.

For the beam tests, single-sided assemblies were built using prototype ceramic hybrids for interconnections between APV5 chips and connections to the driver electronics board. These were subsequently installed at CERN. The driver electronics, the APV5's and the LED based opto-electronics links were supplied by RAL. The mechanics and assembly were provided by RAL and QMW with hybrids designed at Liverpool and fabricated by CERN. Detectors were tested at RAL, Cambridge and Liverpool and wire-bonded into the modules at RAL. At the start of the test-beam period, the same electronics and read-out were employed to test a 12cm length pair of forward $p-$strip fan geometry detectors[7], giving a signal/noise at the peak of the Landau distribution of 14:1 (no deconvolution). This system was also used to test operation with Multi-Quantum Well (MQW) read-out using a system provided by Birmingham and no adverse affect on the performance could be detected[14,15].

In a special test run, the optical fibres for transmitting the clock and control data to the module were replaced with the Oxford prototype of the ATLAS system for transmission of timing, trigger and control data to the front end modules. In this system pulse height modulation (PHM) is used to send clock and control data down a single fibre. The system was operated successfully and more details are available in ref [16].

This programme was, however, hindered by the difficulties of yield and performance of the APV5 chips. No chips performed at the design clocking speed and this meant that the deconvolution mode of operation (needed to recover the signal in a single beam-crossing at the LHC) could not be employed. Peak mode (sampling the output of the slow shaper without using the weighted sum technique to recover the fast front-end response) was the only mode available so the measurements were not those appropriate to full speed operation. In addition, the tuning of the front-end performance of these chips was very delicate and it is probable that the operation was not fully optimised for the negative signal expected for an $n-$strip detector. Nevertheless, this read-out did function sufficiently for a full system test of the z-module concept.

Two complete such modules were assembled and tested, although it proved impossible to equip these with their full compliment of APV5 read-out chips. However, the construction of such modules and their operation has been demonstrated and no results to date suggest that these modules would not perform to the ATLAS requirements given a further iteration of the micro-electronics.

6 Results Using FElix-128 Read-Out

A parallel development to the APV5 is the FElix programme which initiated the development of the pre-amplifier and shaper, analogue pipeline and analogue signal processor architecture[5]. This also continues as a non-radiation hard implementation in which fast turn around allows for quick developments. Many fruitful design concepts have resulted from this programme and the current full size version of this chip does work at the correct clocking speed, allowing both peak and deconvoluted data to be taken. The chips have been designed at Oslo and at CERN and are fabricated in non-radiation hard technology by Austria Mikro Systems (AMS).

In the beam, data were taken with 6cm long, FoxFET biassed, 350μm thick detectors of 50μm read-out pitch fabricated by CSEM (Switzerland). Figure 3 shows the peak mode operation response of such an assembly in units of the single-strip noise, giving a signal/noise at the Landau peak of 33:1. A resolution of 4.6μm at a read-out pitch of 50μm was obtained. In deconvoluted mode, signal/noise values of 15 and 11 were measured for 6cm and 12cm strip lengths respectively. For 6cm strips, a preliminary resolution of 9.1μm was measured. Efficiencies of 99.8% (peak) and 98.9% (deconvoluted) with noise hit probability at $< 10^{-4}$ were obtained with a simple clustering algorithm cutting on both the single strip and cluster significance.

The CERN group were also able to demonstrate the use of MQW read-out with this higher performance electronics and, as for the earlier tests, the MQW

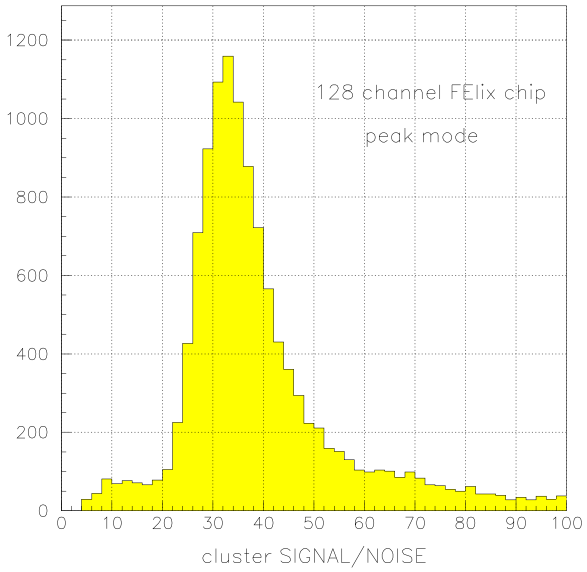


Fig. 3. *Pulse height in units of signal/noise for the FElix-128 chip reading out a 6cm AC-coupled FoxFET biassed 50μm pitch, 350μm thick silicon detector.*

read-out is shown not to compromise the performance once the effect of AC coupling the signal is taken into account[15].

Despite a very tight schedule, the CERN and Liverpool groups were able to operate one of the ATLAS design detectors with this electronics. Whilst subsequent testing suggests the front-end may not have been tuned optimally for negative signals, a signal/noise of 17 (peak) and 11 (deconvoluted) was obtained in beam with a 6cm length, 300μm thick device. The resolution figures of 12.8μm (peak) and 15.7μm (deconvoluted) (figure 4) both demonstrate the advantages of an analogue read-out scheme which gives resolution $\ll$ (pitch=112.5μm)/$\sqrt{12}$. Figure 5 shows how the collected charge (in units of the strip noise) differs for tracks extrapolating to a read-out strip compared with tracks extrapolating to the intermediate strip. Whilst some charge loss is seen (particularly for the peak data), this is at an acceptable level for the deconvoluted data ($\sim$ 10%). This shows that the intermediate strip is effective for charge division in such a design and screening by the surrounding $p-$isolation frame is not a concern. The efficiency with a cut on the cluster signal of four times the noise is $\geq$ 99.5% in both peak and deconvoluted mode, with a corresponding noise hit probability of $\sim 10^{-4}$.

Future development of this programme involves incorporating the analogue pipeline and multiplexer onto a fast bipolar front-end as part of the development towards the AROW project[6]. It is hoped that this configuration will provide a test bed for irradiated detectors, which employs the correct speed front-end and gives full analogue read-out, allowing a direct assessment of the

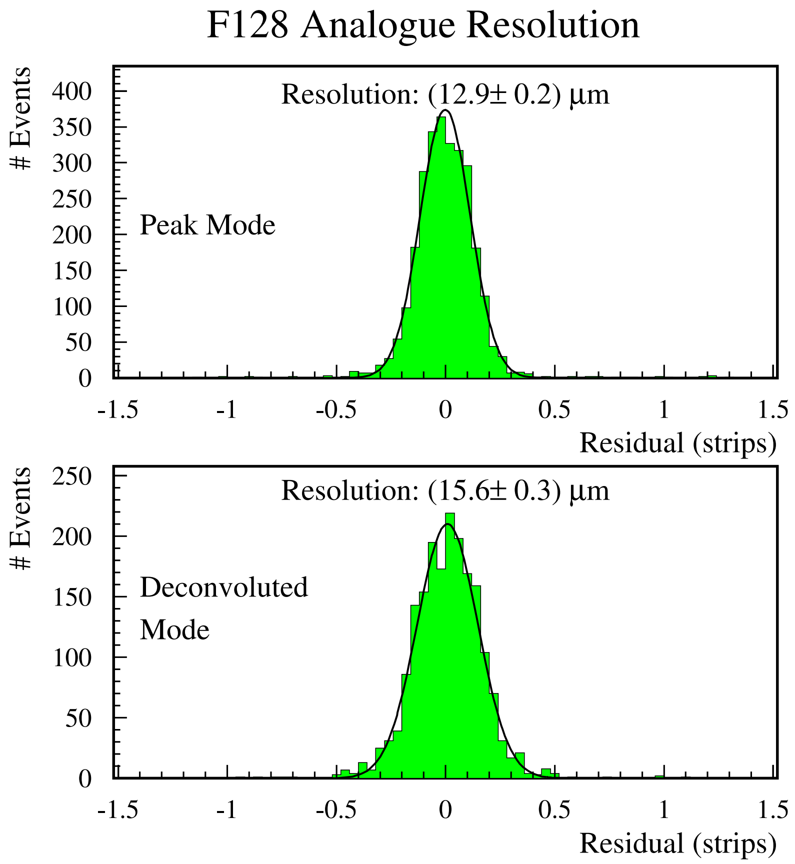


Fig. 4. *Spatial resolution for the ATLAS-A detector (112.5µm read-out pitch) in peak and deconvoluted modes with FElix-128 read-out.*

device performance after radiation damage.

7 Conclusions

Several read-out chips allowing pulse-height information to be transmitted off detector have been tested at CERN. Detectors to the ATLAS specification for $n-$strip in $n-$type silicon were fabricated and tested with two of the available read-out architectures. Measurements with these, and with simpler $p-$strip detectors, demonstrate the advantage in spatial resolution to be achieved with an analogue read-out scheme. However, it has not yet proved possible to demonstrate read-out of 300μm thick detectors, daisy-chained together to give 12cm length, with a signal reconstructed in one 25ns beam crossing giving signal/noise of $\geq$15. Developments with bipolar front-end replacing the current CMOS pre-amplifiers should produce results by the end of 1995 and further progress in 1996 will be made in the context of the AROW

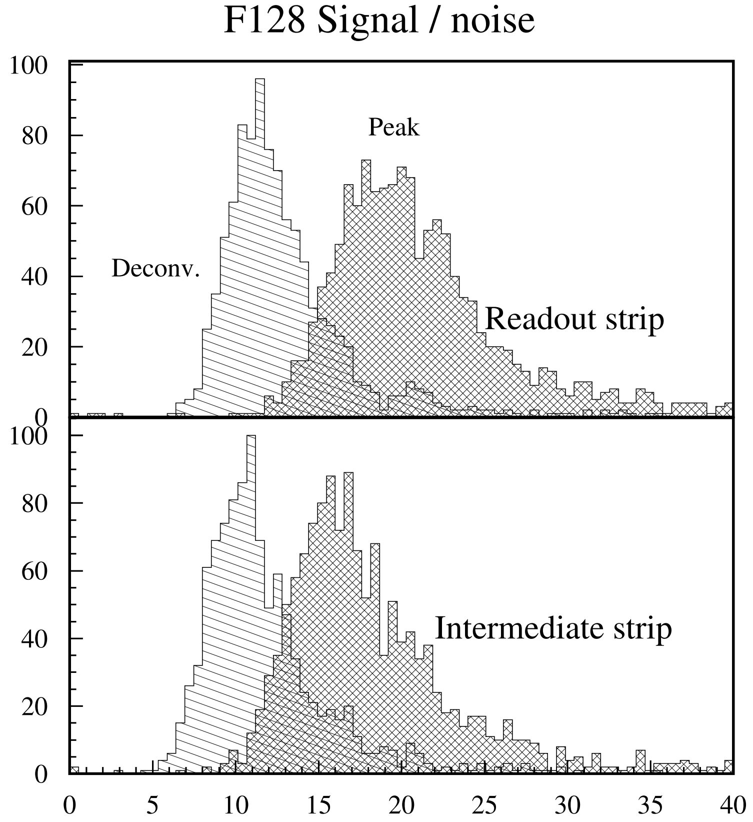


Fig. 5. *Pulse height for the ATLAS-A detector for tracks extrapolating to either the read-out (top) or intermediate strip (bottom) in units of the single strip noise using FElix-128 read-out. The dark hatched distributions show the results for the 'peak' mode of operation while the lighter hatched distributions are for the 'deconvoluted' mode.*

programme. In addition, further development of the existing CMOS architectures is anticipated both within ATLAS and CMS. As ATLAS has set itself the target of a decision on electronics architecture at the end of 1996, these programmes are being aggressively pursued to explore whether either of the schemes allowing analogue information to be recorded can be adopted.

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