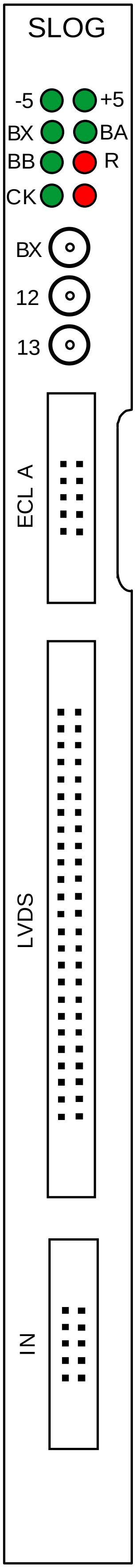
SLOG



1. Overview

SLOG (**SLOw command Generator)** is designed to allow the generation of SLOW Commands for the control and configuration of ATLAS SCT Front-End chips. It fans out Clock and Fast Commands from an external source (CLOAC) together with the internally generated SLOW Commands to 12 channels at LVDS levels for use in Multi-Module electrical test setups. Two copies of the Clock and Command are also output at ECL levels, so that SLOG can drive 2 Oxford Fibre-Optic Drivers, or more if the UCL Fanout module is used. An internal 40 MHz clock may be selected, allowing SLOG to generate clock and commands in stand-alone mode.

Fig1 shows the main features of SLOG. The slow commands are assembled by a host computer, loaded to a ram and then output synchronised to the clock. There are 3 14-bit Output Enable Registers which allow each channel to have Clock, External Command and Internal Command separately enabled. Figs 2 and 3 show how SLOG might be used in the System Test and in a multi-module test rig.

A batch of 4 SLOGs has been manufactured. The SLOG design has now (27-June-99) been modified to give computer control of the clock duty cycle and of the phase relationship between clock and data. The new design is fully compatible with the old one and can replace it without software change. The additional functions of the new design will be described later in this document.

1.1. Format

SLOG is a 6U single-width VME module. It is an A32 or A24 module, the mode being selected by means of a jumper. All transfers are D16, programmed. Block transfer is not supported. The base address is selectable by 4 hex switches for the A32 mode and by the least significant 2 of these switches for the A24 mode. SLOG responds to AM codes 9,A,D and E in A32 mode and 39,3A,3D and 3E in A24 mode. All transfers are 16-bit, aligned to even byte boundaries. SLOG occupies 128 Kbytes of VME address space. DTACK is asserted for any valid operation to this space. BERR is never asserted.

1.2. power requirements

SLOG requires +5V and –5.2V .

The -5.2V may be provided via the *JAUX* connector if used in a CERN standard crate or via the J2 connector if used in a normal VME crate. In this case the user has to provide -5.2V and 0Vat the appropriate J2 pins. These are: -5.2 at C4, OV at C3,C7 and C10. Jumpers must be inserted in PL8,9,10 and 11. When jaux is used, the jumpers may be removed to isolate the J2 pins.

1.3. Front Panel Connectors

A 10-pin header connects the 2 differential ECL inputs, Clock and Control

A 50-pin header carries the 24 differential LVDS outputs, 12 pairs of Clock and Command

Two 10 pin headers each carry a copy of clock and command from channels. They also carry Busy inputs, which allow SLOG to drive 2 MuSTARDS in a stand -alone mode.

There are 3 lemo sockets.

One Input, NIM, external busy, this input can be used to inhibit SLOG cycles.

Two outputs, these carry the outputs of memory bits 12 and 13. These can be programmed and used as desired.

50 pin header

clock0	1	2	clock0b
clock1	3	4	clock1b
clock2	5	6	clock2b
clock3	7	8	clock3b
clock4	9	10	clock4b
clock5	11	12	clock5b
clock6	13	14	clock6b
clock7	15	16	clock7b
clock8	17	18	clock8b
clock9	19	20	clock9b
clock10	21	22	clock10b
clock11	23	24	clock11b
com0	25	26	com0b
com1	27	28	com1b
com2	29	30	com2b
com3	31	32	com3b
com4	33	34	com4b
com5	35	36	com5b
com6	37	38	com6b
com7	39	40	com7b
com8	41	42	com8b
com9	43	44	com9b
com10	45	46	com10b
com11	47	48	com11b
gnd	49	50	gnd

10 pin front-panel header ECL_A

BUSY (in)	1	2	BUSYb
	3	4	
	5	6	
clock12 (out)	7	8	clock12b
com (out)	9	10	comb

10 pin header (behind front-panel) ECL_B

BUSY (in)	1	2	BUSYb
	3	4	
	5	6	
clock13 (out	7	8	clock13b
com (out)	9	10	comb

10 pin header INPUT

	1	2	
	3	4	
	5	6	
clock	7	8	clockb
com	9	10	comb

1.4. Front Panel LEDs

LEDs indicate the presence of 5V and –5.2V.
The states RUN, External Busy, BusyA and BusyB (BX,BA,BB).
The presence of the clock. This led is lit if a clock is present, whether internal or external.
The bottom right led is not used.

2. VME functions

Jumper PL3 controls the A24/A32 function.
When present the module is A24, when absent it is A32.

2.1. Start/Stop

Base Address. read, write
D0 Start when 1, stop when 0.
When reading, D0 indicates RUN. D3:1 will be zero, D15:4 will be undefined
RUN is true from Start until the last of the requested cycles has finished.

2.2. Start Address Register

Base Address + 2. read, write
D 14:0 Start Address
This register provides the memory address at which a slow command cycle starts.
When read, D15 is zero.

2.3. Cycle_count

Base Address + 4 read, write
D15:0 After Start, memory cycling will continue until this count decrements to zero,ie the number of cycles executed will be cycle_count + 1.
The count is decremented by the STOP_BIT. If the cycle_count is loaded with zero then one cycle of the memory is output, and the count remains at zero.

2.4. Busy Enables

Base Address + 6 read, write.
D2:0
If running SLOG with multiple cycles, then a BUSY may be asserted to pause the cycles. There are 3 sources of BUSY, BUSYX from the front-panel Lemo socket or the BUSY inputs on the 10-pin ECL headers (which would be used only if MuSTARD was being driven directly by SLOG). These are BusyA (the front-panel header), and BUSYB (the header located on the board behind the A header)
D0 = 1 enables BUSYA, D1 = 1 enables BUSYB and D2 = 1 enables BUSYX.
When read, D6 indicates the state BUSY which is the or of the states at the 3 BUSY inputs, D5:3 the states of the busy inputs X,B and A, and D2:0 show the state of the busy enables. D15:7 will be zero.

2.5. Clock Enable Register

Base Address + 0x10. read, write.
D13:0 Each bit enables the clock output for the corresponding channel. Bits 11:0 enable the LVDS outputs, bit 12 enables ECL_A, bit 13 enables ECL_B. Note that if either Clock_Enable 12 or 13 is zero, the corresponding COM output at ECL_A or ECL_B will also be zero.

2.6. External Command Enable Register

Base Address + 0x12, read,write.
D15:0 Each bit enables the external command output for the corresponding channel, ie it enables the external command input to be routed to the corresponding output channel ORd with the corresponding internally generated command. Bits 11:0 enable the LVDS outputs, bit 12 enables ECL_A, bit 13 enables ECL_B, bits 14 and 15 enable the LEMO front-panel outputs.

2.7. Internal Command Enable Register

Base Address + 0x14 read, write.
D15:0 Each bit enables the internal command output for the corresponding channel. Bits 11:0 enable the LVDS outputs, bit 12 enables ECL_A, bit 13 enables ECL_B, bits 14 and 15 enable the LEMO front-panel outputs.
Note that for the LVDS channels the enables are independent, that is each channel may have its clock enabled or disabled independently of data, and internally generated command data and externally generated command data may be independently enabled.
ECL Output Select registers.
There are 2 4-bit registers which allow data from any of the memory channels 0:14 to be multiplexed to the ECL outputs.
GMR_A
Base Address + 0x16
D3:0
GMR_B
Base Address + 0x18
D3:0

2.8. COMMAND RAM

32K * 16 located at Base Address + 0x10000 Read, Write

Address Map

hex	
0	start-stop register
2	Start address register
4	Cycle_count
6	Busy register
10	clock enable register
12	external output enable
14	internal output enable
16	gmr_a
18	gmr_b
20	clock control register SLOG B only
10000	SLOG Memory
1fffe	

3. Operation Guide

The heart of SLOG is the 32K * 16 RAM, to which 15 separate slow command strings may be written, ie each of the 15 bits (0:14) is an independently programmable channel. The RAM may only be written or read when RUN, the state in which the RAM is outputting its data as command strings, is not asserted. Run may be de-asserted by writing to the Stop/Start Register with D0 = 0.

Bits 11:0 of the RAM correspond to the 12 LVDS channels output on the 50-way idc header.

Bits 12 and 13 are output at NIM levels on front-panel Lemo sockets. These may be used as markers or scope triggers or whatever.

2 channels are output at ECL levels, each on a 10-pin header, these channels are referred to as ECL_A and ECL_B. Each of these channels may be fed by any one of the 15 memory channels

Bit 15 of the RAM is the STOP_BIT which should be programmed with zeroes until the end of the command string, then a 1 should be written.

Writing to the Start/Stop register with D0 = 1 starts the outputting of the command strings, with RUN being asserted. The address for the RAM during RUN is provided by a 15-bit address counter, incremented by the 40 MHz (or BC) clock. When RUN commences, the contents of the START_REGISTER are loaded to the address counter which then counts up from that value until the STOP_BIT is asserted. If the CYCLE_COUNTER is zero, RUN is cleared by the STOP_BIT. If the CYCLE_COUNTER is not zero then RUN remains asserted, the START_REGISTER contents are loaded to the address counter, the CYCLE_COUNTER is decremented and another RAM cycle begins. If bit 15 of the CYCLE_COUNTER is set then this counter is not decremented ie the command sequence is output continuously until a zero is written to the Start/Stop Register. If the STOP-BIT is not programmed, then after RUN starts the address counter continues to increment, wraps round to zero and the sequence continues indefinitely until a zero is written to the Start/Stop Register.

If single cycles are required, then the CYCLE_COUNTER should be loaded with zero. The counter will not be decremented , and so more single cycles may be initiated just by writing to Start. Note that since there is complete flexibility in programming the command memory, SLOG may be useful for generating fast commands in certain cases, for example it can be used to generate bursts of L1 triggers, or L1 triggers following slow commands etc.

All command strings should begin with at least 2 zeroes.

3.1. The Enable Registers

The 3 enable registers enable Clock, External command and Internal command. If both Internal and External is enabled for a channel then the OR of the Internal and External commands is output. Bits 11:0 of the enable registers affect the 12 LVDS outputs, bits 12 and 13 enable the ECL_A and ECL_B outputs. Bits 14 and 15 enable the NIM outputs at the front-panel Lemo sockets, but the internal signals for these sockets come from bits 12 and 13 of the memory. This may seem a bit unnatural, but it does allow the NIM outputs to be enabled independently of the ECL outputs. The NIM outputs are useful diagnostic aids. They may be programmed as the user wishes - I find it useful to have a copy of the command sequences output at channel 12, with channel 13 programmed as a scope trigger, thus allowing the scope to be triggered at a precise point in a complex set of commands. In the case of the ECL outputs the data outputs are disabled if the corresponding clock enable bit is not set. In the case of the LVDS outputs clock enable, internal enable and external enable are completely independent.

3.2. The ECL select registers

There are 2 registers, GMR_A and GMR_B. Each is 4 bits, GMR_A selects a memory channel to output at ECL_A, GMR_B selects a memory channel to output at ECL_B. Any memory bit may be selected except bit 15, used as the stop bit.

3.3. Stand-Alone Operation

In order to give SLOG some standalone capability either for test purposes or for those setups where the full functionality of CLOAC is not required an internal 40 MHz clock is provided. To use this clock, 2 jumpers should be inserted in PL14 as shown in fig 2

The 2 ECL output headers can drive MuSTARD, and receive BUSY from them. This may enable SLOG to operate in standalone mode in small electrical test setups.

3.4. Clock Duty Cycle

The Clock duty cycle may be adjusted by an internal hex switch. This must be calibrated by observing the output clock preferably at the output of a receiver, eg on the support card. The 2nd version of SLOG allows computer control of the clock duty cycle, see the later description.

3.5. Use in the System Test and Multi-module electrical test setups

Fig 3 indicates what I believe would be a reasonable setup for use in the System Test until ROD99 becomes available. The items in black indicate what I expect to be at CERN in 98, with the items in grey being added in 99 as required. CLOAC provides the Clock, and CLOAC and SLOG provide the Commands. One of SLOG's ECL outputs is used to drive up to 4 Oxford Fibre-Optic Drivers via a UCL Fanout unit. The FODs are used in transparent mode ie they use external CLOCK and COMMANDs. The COMMANDs are routed to particular detector modules by using the OUTPUT ENABLE registers in the FODs. See the Oxford Fibre Optic Driver Operating Manual.
Fig 4 indicates how SLOG might be used with MuSTARD and CLOAC in a multi-module electrical test setup.

4. SLOG B

SLOG has been redesigned to permit its use in the SCT OPTO-HARNESS Test System.
The new version powers up in a mode which is completely compatible with version A, and no software changes are needed.
The new facilities are that the clock duty cycle may be programmed, as can the phase between the command data and the clocks.
To do this, a new register, CLOCK_CONTROL has been included at Base-address + 0x20.
This is a read-write register with the following functions.

CC0 When zero the default setting of the clock duty cycle is used, ie the duty cycle is determined by the internal hex switch. When 1, the clock duty cycle is set by CC7:4. These bits are applied to a 4-bit programmable delay unit which shifts the falling edge of the clock in steps of 400 pS.

CC1 When zero, the phase of the LVDS COM outputs relative to the LVDS CLOCK outputs is the default value. The default value is such that data changes approximately 12 nS before the rising edge of the clock. When 1, the phase is set by CC12:8. These bits are applied to a 5-bit programmable delay unit which shifts the clock in steps of 1 nS.

CC2 When zero, the phase of the ECL_A COM output relative to the ECL_A CLOCK output is the default value. When 1, the phase is set by CC12:8.

CC3 When zero, the phase of the ECL_B COM output relative to the ECL_B CLOCK output is the default value. When 1, the phase is set by CC12:8.

CC7:4 Control the programmable clock duty cycle

CC12:8 Control the programmable phase of COM relative to CLOCK.

When CC0 is 1, then when CC is read, the value of the CLOCK_CONTROL register is read, with bits 15:13 being zero.
When CC0 is zero, then when CC is read bits 15:13 are zero, bits 12:8 and bits 3:0 are the CLOCK_CONTROL register bits, but bits 7:4 are the setting of the clock duty_cycle hex switch. Fig n makes this clear.
A word of caution: The clock duty cycle may be varied from approximately 40:60 to 60:40. The falling edge of the clock can be moved in 400 pS steps. This is achieved by using a 4-bit programmable delay unit. These devices are guaranteed monotonic, but any one step size can vary between 0 and 800 pS. Users of this function (ie those using electrical readout; those using fibre-optic readout will not be concerned with clock duty cycle) are strongly urged to monitor the clock duty cycle as close as possible to the point at which the clock is used.
The ability to vary the phase of the clock relative to the data was designed specifically for fibre-optic harness testing and would not be expected to be used in module testing. Fig 5 shows that the clock is delayed by a programmable delay unit (32 steps of 1 nS). This delay unit will ouput a clock whose duty cycle is not precisely defined and which will be a function of the delay. Beware!

Identification
Visually: SLOG B has 6 hex switches. SLOG A has 5. It also has a serial number beginning with B.
By Software: SLOG B powers up with CC3:0 set to zero, bits 12:4 undefined. When CC3:0 = 0 the other bits of CC have no effect. As part of SLOG initialisation write 0x15X0 to CC, then read it back. If the value read = 0x15X0 then you have SLOG B.
In the case of both SLOG A and SLOG B the firmware version can be read. There are 3 PALs known as SLA, SLD and SLV. The firmware version for SLV can be read at BASE_ADDRESS + n (only the least significant 5 bits are defined). The version for SLA is at BASE_ADDRESS + nn and for SLD at BASE_ADDRESS + nnn. These version numbers are not normally significant, but in the event of a problem report it would be helpful if they could be quoted.

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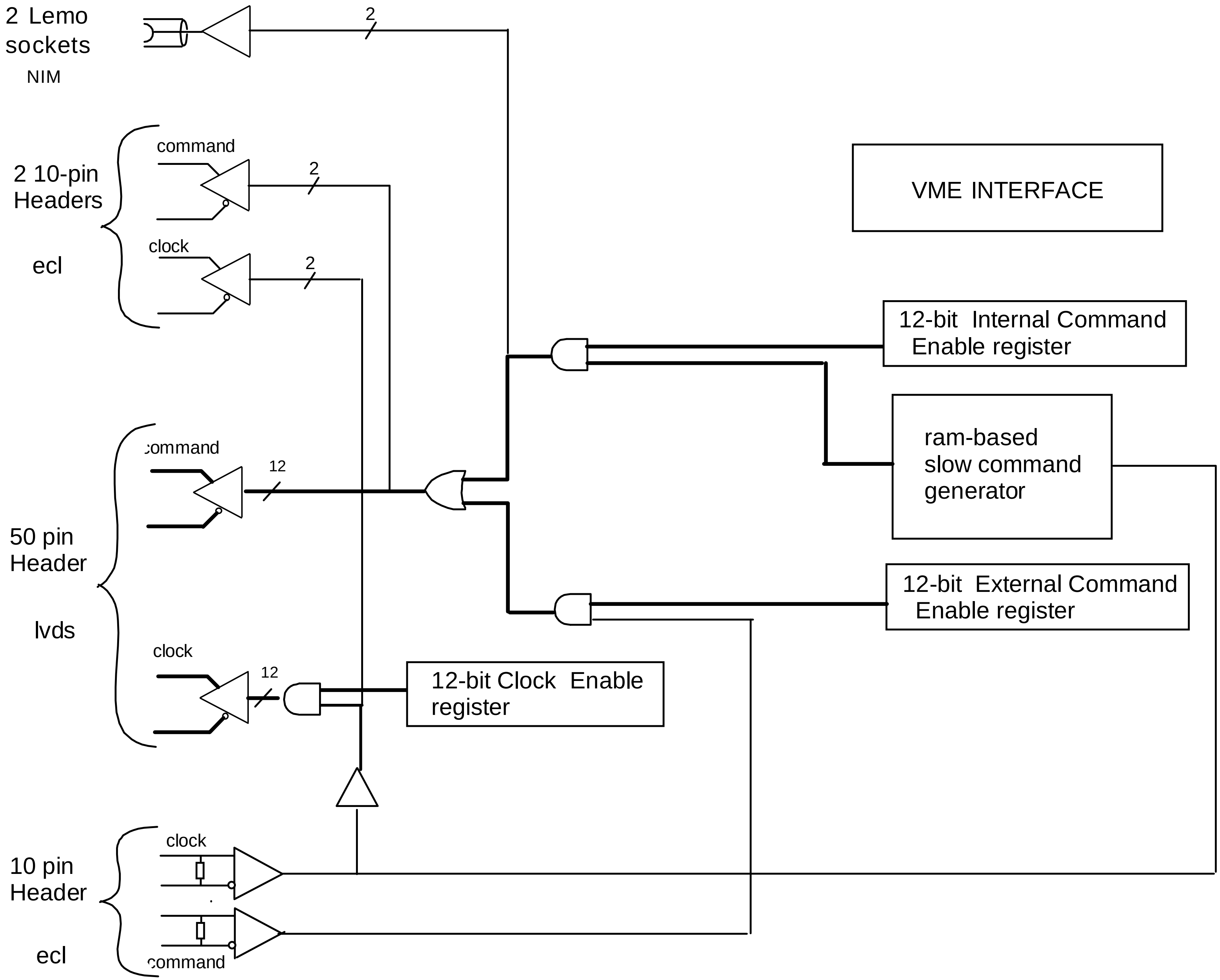
2 Lemo
sockets
NIM
2
2 10-pin
Headers
ecl
command
2
clock
2
VME INTERFACE
12-bit Internal Command
Enable register
ram-based
slow command
generator
command
12
50 pin
Header
lvds
12-bit External Command
Enable register
clock
12
12-bit Clock Enable
register
clock
10 pin
Header
ecl
command

fig 1

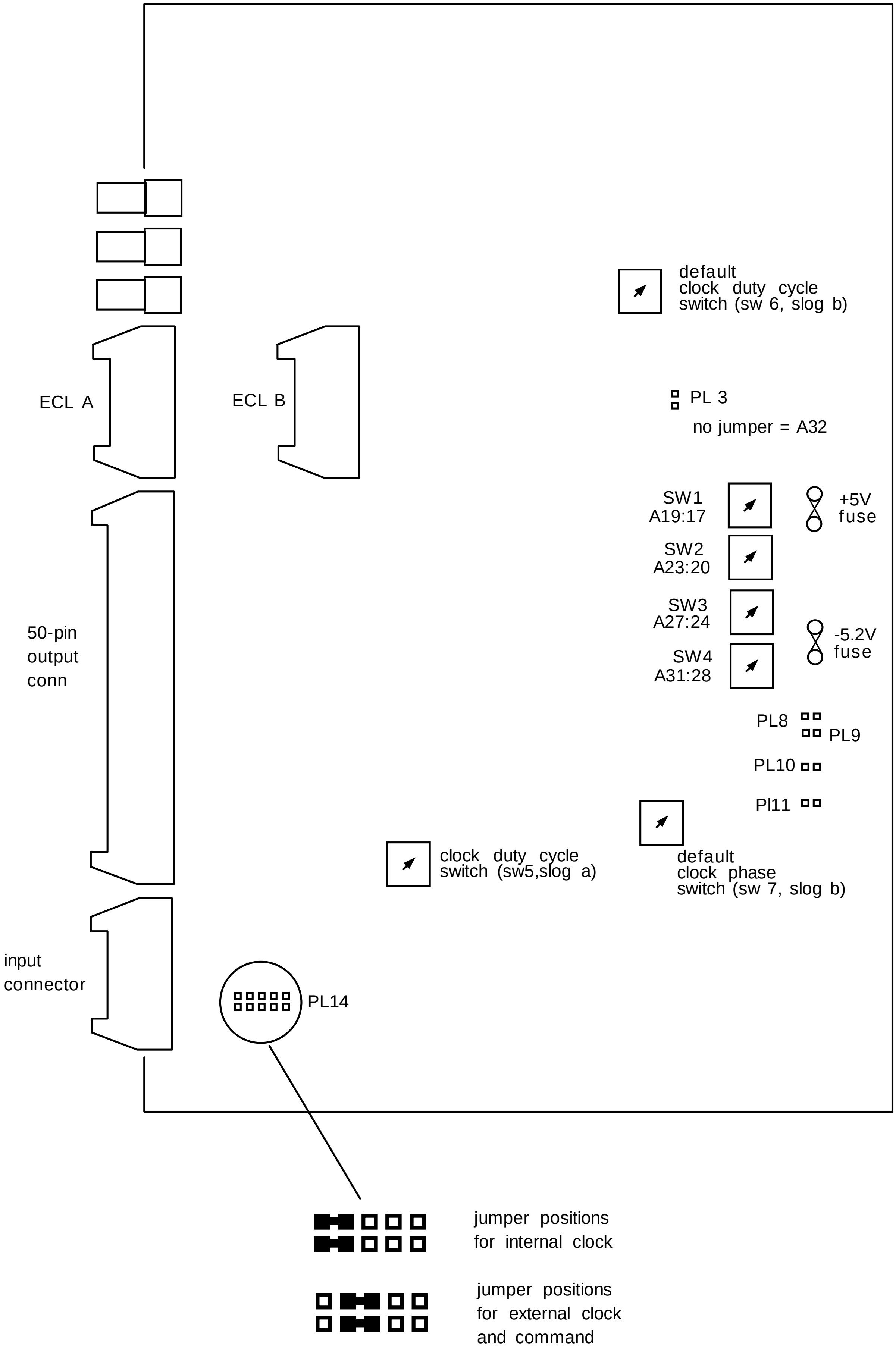
default
clock duty cycle
switch (sw 6, slog b)
ECL A
ECL B
PL 3
no jumper = A32
SW1
A19:17
SW2
A23:20
SW3
A27:24
SW4
A31:28
+5V
fuse
-5.2V
fuse
50-pin
output
conn
PL8
PL9
PL10
Pl11
clock duty cycle
switch (sw5,slog a)
default
clock phase
switch (sw 7, slog b)
input
connector
PL14
jumper positions
for internal clock
jumper positions
for external clock
and command

fig 2

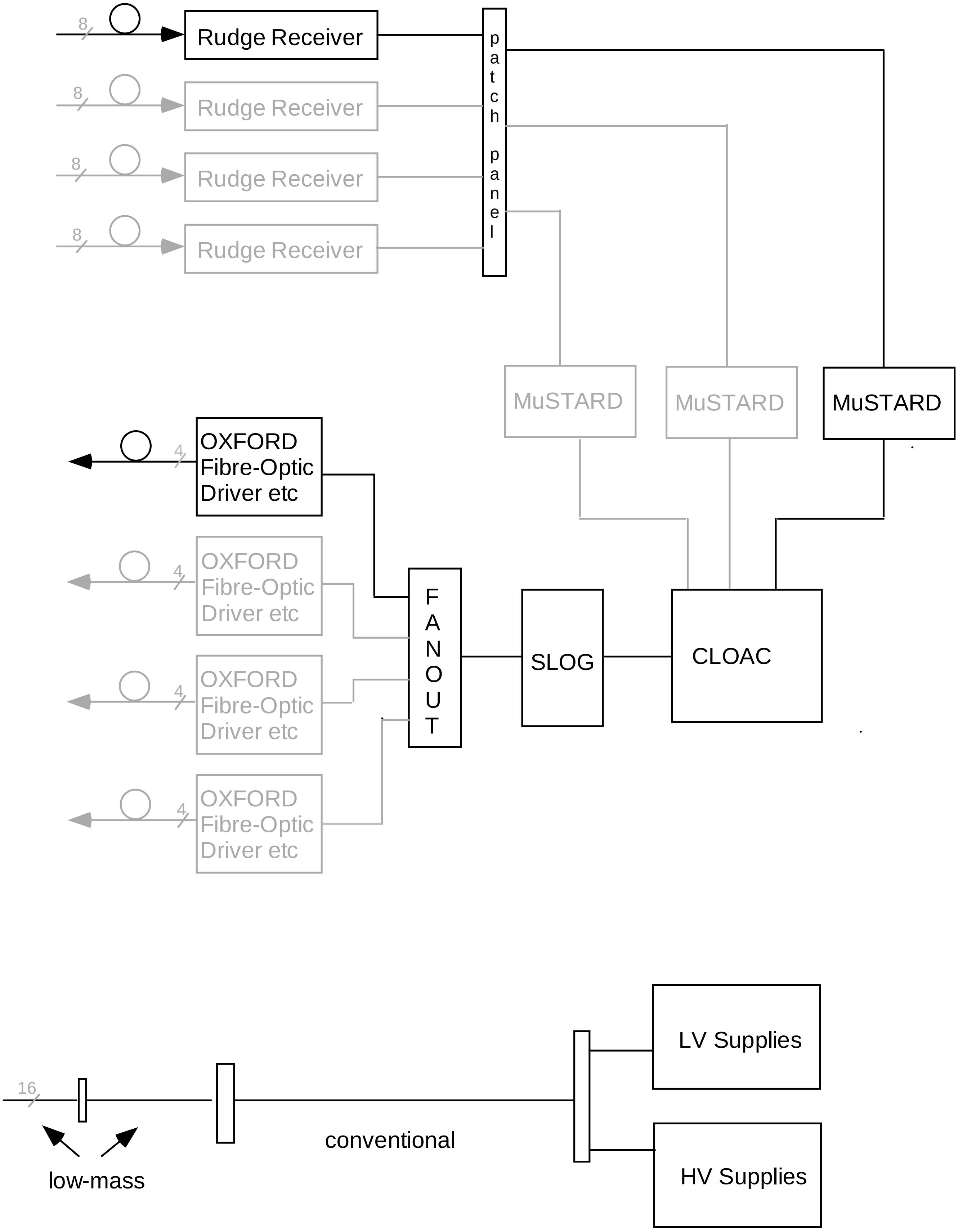
8
Rudge Receiver
8
Rudge Receiver
8
Rudge Receiver
8
Rudge Receiver
patch panel
MuSTARD
MuSTARD
MuSTARD
4
OXFORD Fibre-Optic Driver etc
4
OXFORD Fibre-Optic Driver etc
4
OXFORD Fibre-Optic Driver etc
4
OXFORD Fibre-Optic Driver etc
FANOUT
SLOG
CLOAC
16
low-mass
conventional
LV Supplies
HV Supplies

fig 3

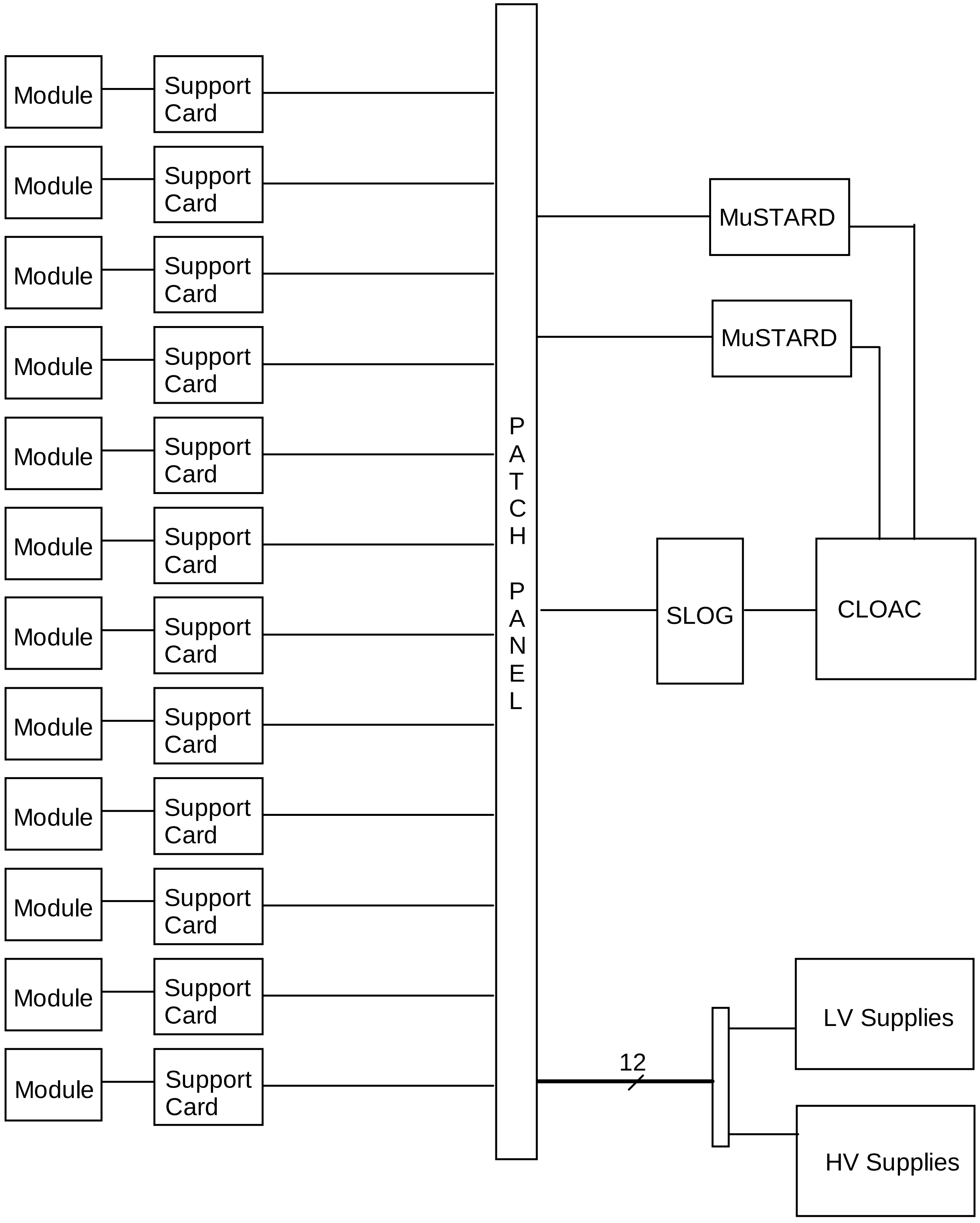
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
Module
Support Card
PATCH PANEL
MuSTARD
MuSTARD
SLOG
CLOAC
12
LV Supplies
HV Supplies

fig 4

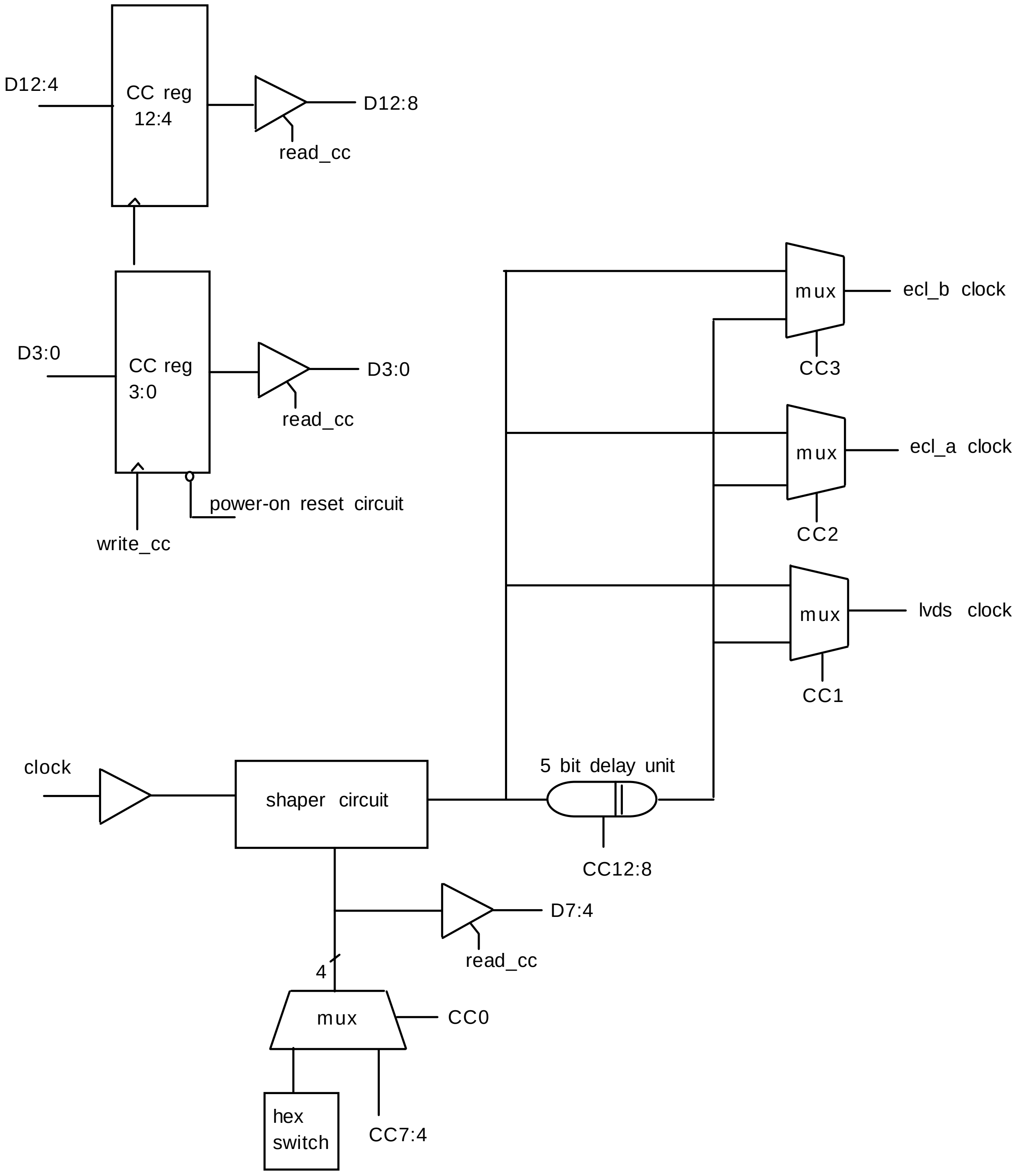
D12:4
CC reg
12:4
D12:8
read_cc
D3:0
CC reg
3:0
D3:0
read_cc
power-on reset circuit
write_cc
mux
ecl_b clock
CC3
mux
ecl_a clock
CC2
mux
lvds clock
CC1
clock
shaper circuit
5 bit delay unit
CC12:8
D7:4
read_cc
4
mux
CC0
hex
switch
CC7:4

fig 5