13 Common Inner Detector Electronics

13.1 Overview

The overall electronics, readout, and control system for the ID is shown schematically in Figure 13-1. It consists of two major parts: the *front-end* or *on-detector* electronics, which is mounted on the detector modules, and the *back-end* or *off-detector* electronics which is located in USA15 and in the counting room. The front-end electronics performs the requisite signal processing and storage in the Level-1 pipeline for each type of detector and is largely specific to the Pixel (Section 10.4), SCT (Section 11.4), or TRT (Section 12.8) sub-systems. Common issues here concern primarily (1) the need for radiation hard technologies, discussed generally in Section 13.2 below, (2) the data, timing, and control links between the on-detector and off-detector electronics, and (3) the philosophy for grounding and power distribution. Two different types of links are being considered: shielded twisted pair, discussed in more detail in Section 12.9.1.2, and optical links, discussed in more detail in Section 11.4.6. These links are envisaged to operate at 40 MHz except for the readout of the Pixel B-layer where 80 MHz links are being considered. An effort is being made to ensure as much commonality as is possible, but both twisted pair and fibre links may be utilised depending on the needs of the individual systems. Initial guidelines for grounding and power distribution are discussed below in Section 13.3.

The off-detector electronics is comprised of the readout system, which will link the front-end electronics modules to the ATLAS Trigger and Data Acquisition (Trigger/DAQ) system and to the ATLAS timing and trigger control system (TTC), and the power supplies and local detector control system (DCS) for slow control and monitoring. The readout system provides timing and control signals to the front end with timing information distributed to a precision of 0.5 nsec. In response to a trigger, it reads event data from the modules and must function with minimal deadtime up to the ATLAS LVL1 trigger rate of 75 kHz. The system must be partitionable such that subsets of the electronics can provide data acquisition needs during fabrication of the detector modules and such that different portions of the ID can operate autonomously during the commissioning and debugging phase of the detector.

To accomplish these functional and performance requirements, the off-detector readout and control system will be crate based and modular, employing existing data acquisition standards, but utilizing custom components where essential. Individual elements of the system will be similar, (although not always identical due to the differing requirements) for the Pixel, SCT, and TRT detectors. The basic elements are:

Crate, Backplane, and Readout Controller. The modular design of the readout system will employ standardised crates, such as 9U x 400mmVME, utilizing the new VME-P standard where necessary. The crate backplane will not be utilised for high bandwidth data acquisition; the high-speed data paths will be via standard ATLAS Readout Links directly to the Readout Buffers (ROB) in the ATLAS Trigger/DAQ system. The crate backplane, however, will be used for low bandwidth data acquisition in laboratory and debugging contexts and for data monitoring, on a sampled event basis, during normal operation. The crate backplane will be the sole control path for the readout and control electronics.

The readout controllers (ROC) in each crate will be commercial single board computers running the standard ATLAS real-time operating system such as LynxOS. They will be responsible for

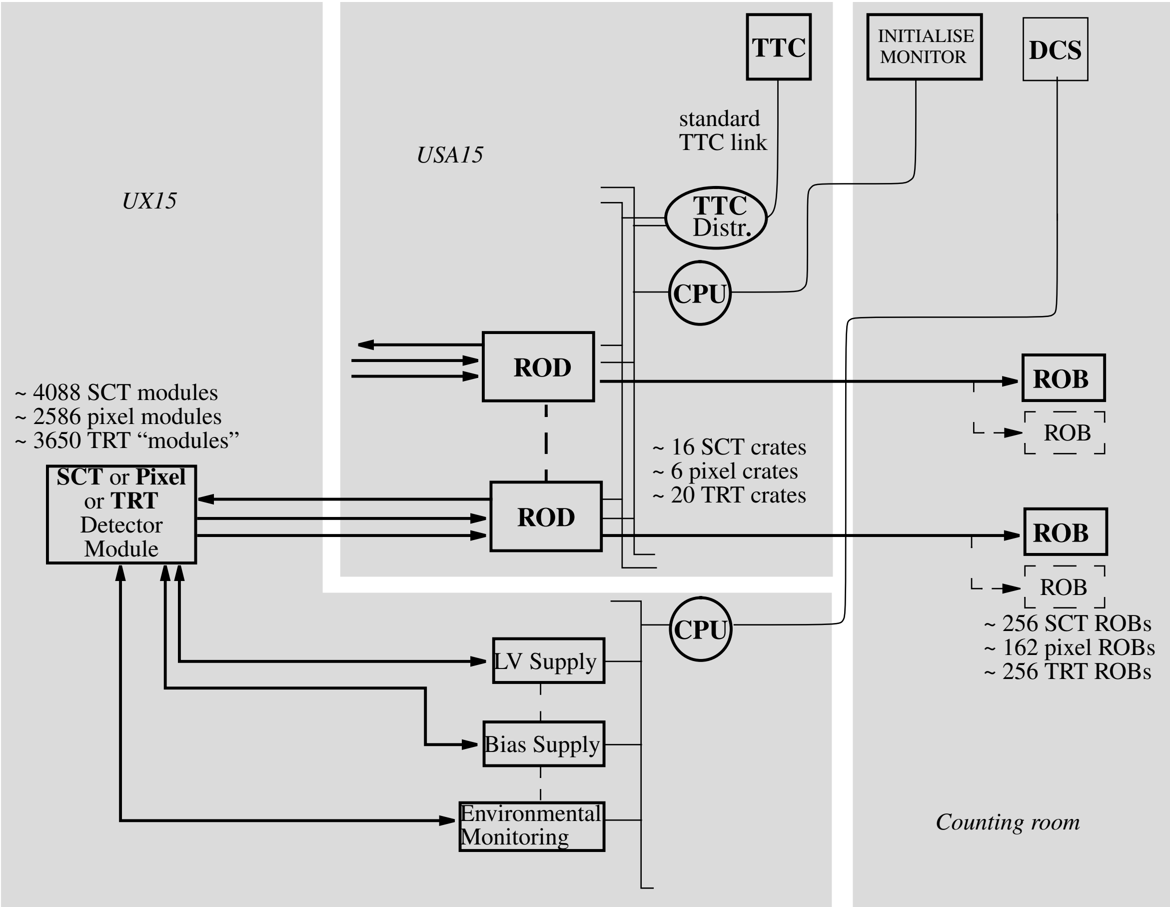

Figure 13-1 Schematic Inner Detector readout and control system.

configuration and control of the readout modules and the front end electronics. The ROC is also the principal interface to the ATLAS DAQ for control purposes, via a local area network.

The Trigger, Timing, and Control (TTC) distribution module. This module is located in the readout crate, receives the basic timing and trigger information from the central ATLAS TTC system, and distributes the clock, trigger and bunch counter information to the front end electronics and to the ROD; signals to the latter will be transmitted via a custom crate backplane. The physical distribution of the TTC signals must be somewhat different for the TRT than for the Pixel/SCT sub-systems because of the different modularities.

The readout driver modules (ROD) which read data from the front end circuits, provide first level data collection, error checking, zero-suppression, formatting, and buffering and then ship the data to the ReadOut Buffers (ROB) over high speed links. The ROD's will also allow data monitoring (on a sampled event basis), and data acquisition during the early periods when the ROB's are not available, via the crate microprocessor board. Interfaces on the ROD, such as to the ROBs and local crate controller will be standardised, but specific implementation of data collection and zero-suppression will be different for the Pixel, SCT, and TRT subsystems.

The Readout Buffer Modules (ROB) These modules, as well as the links from the RODs to the ROBs, will be common to all the Atlas sub-detectors. The ROBs are the data source for both the Level-2 and Level-3 trigger systems.

Detector Control System (DCS) This system is responsible for slow control of the experiment, e.g. the setting of low and high voltages, and for monitoring various environmental factors such as temperatures, pressures, gas flows, etc.

DAQ LAN The readout and control electronics will be interconnected by a dedicated local area network (LAN), which will also connect to the ATLAS Trigger/DAQ system. This network links ROCS in each readout and control crate with workstations which control and coordinate operation of the readout system. Either the same LAN, or a similar one, will provide connection between the readout system and the local Detector Control System to the ATLAS wide DCS which will be used to control and monitor various voltages, temperatures, pressures, etc.

The modularity, functional requirements, and development plans specific to the readout systems for the Pixel and SCT are presented in Section 13.4.1 and those for the TRT in Section 13.4.2. Discussion of the DCS system is presented in Section 13.5.

13.2 Radiation Damage

Given the radiation levels foreseen for the Pixel, SCT, and TRT detectors, radiation hardened front-end chips are required for operation of the front end electronics. The front end chips will thus be fabricated in radiation hard processes and the technological options being considered are driven by availability of adequate processes. Our present concept of front end electronics for the SCT and TRT relies on two types of processes, bipolar for the analogue front end circuitry and CMOS for the pipeline, control and back end readout circuitry. For each of these subsystems, as discussed in Sections 11.4.4 and 12.8.1, one option consists of two independent chips, one bipolar and one CMOS, while a second option consists of a single BiCMOS circuit. As noted in Section 10.4, the Pixel electronics development also pursues two options, one of which uses only CMOS integrated circuits and one of which requires a BiCMOS process. Thus all three detector systems have readout options which do not require a rad-hard BiCMOS process. While at least one such process does exist, that of DMILL, the designs not requiring BiCMOS enable a substantially wider pool of possible foundries. A summary of the required radiation hardness for each of the Pixel, SCT, and TRT systems is presented in Table 13-1, along with a very condensed summary of the present level of radiation tests that have been conducted on the primary integrated circuits required for each sub-system.

We discuss in more detail below the radiation hardness of bipolar transistors and of CMOS transistors considering in particular the bipolar processes from MAXIM and DMILL and CMOS processes from Honeywell and DMILL. As already noted, for the DMILL technology both types of transistors are available in the same BiCMOS process. We note that there are other radiation hard processes available, e.g. AT&T and Harris for bipolar and Harris for CMOS, as well as others. However, we limit our discussion here to MAXIM, Honeywell, and DMILL.

13.2.1 Bipolar Junction Transistors

The concept of using bipolar transistors for the analogue front end circuitry is based on the fact that one can obtain a larger transconductance, and hence lower noise and higher speed for large detector capacitances, at a lower current than for CMOS devices. In addition, many modern bipolar processes are intrinsically quite radiation hard, which opens the possibility of using commercial processes. The radiation effects which do exist in bipolar transistors, although significant at large doses, are often predictable and can be taken into account in the design. The

Table 13-1 Required radiation hardness for the Pixel, SCT, and TRT systems.

Sub-detector	Requirements		Process	Radiation Tests		
	Ionisation (kGy)	N/cm^2 (10^{14})		Ionisation (kGy)	N/cm^2 (10^{14})	P/cm^2 (10^{14})
Pixel	300	7				
Matrix (FE+RO)			DMILL (96)	**300** (Oct 96)		6
Front End			DMILL (95)	180	7	3.6
MODROC						
LADROC						
SCT	100	3				
CAFE			AT&T (May 95)			**1** (July 96)
CDP 128			Honeywell (93)	**250** (Mar 97)		**> 5** (Mar 97)
SCT32B			DMILL (Mar 96)	**100** (Jun 96)		
SCT128B			DMILL (Dec 96)			
DORIC			AMS (rad-soft)			
TRT	33	1				
ASDBLR			Maxim (95)			**1** (July 96)
DTMROC						
PLL			DMILL (96)			
Tern Rec			DMILL (96)			

main radiation effect is degradation of the current gain factor β which is related to reduction of the minority carrier lifetime in the base region caused by radiation damage. In many modern bipolar technologies, the oxide isolation technique is used, and the carrier lifetime in the base may be limited by surface recombination at the silicon oxide interfaces as well as by bulk recombination. Therefore the β factor is sensitive to both ionisation effects and to displacement damage.

The MAXIM bipolar processes are not considered by the foundry as radiation resistant processes and use of them for the SCT and TRT front end electronics is based on the extensive study of radiation effects in this process which has been performed by the SCT and TRT communities. Bipolar transistors of different sizes have been irradiated at a Co-60 source up to a total dose of 100 kGy in several steps and with a 55 MeV proton beam up to a total fluence of $1\text{x}10^{14}$ p/cm^2. The results show that for this technology the ionising radiation affects the β of bipolar transistors significantly, almost the same way as displacement damage. The current gain factor vs collector current for a transistor with the emitter area of 1.0x7.2 μm^2 after proton and photon irradiation is shown in Figure 13-2 [13-1].

The DMILL process is qualified for radiation hardness up to a total dose of 100 kGy and up to an equivalent 1 MeV neutron fluence of 10^{14} n/cm^2. The radiation hardening includes also bipolar transistors which are available in this process. The design of these devices is optimised for high radiation hardness against displacement damage and ionising radiation. In particular, sensitivity to ionising radiation is reduced by employing radiation hardened oxide structures in the

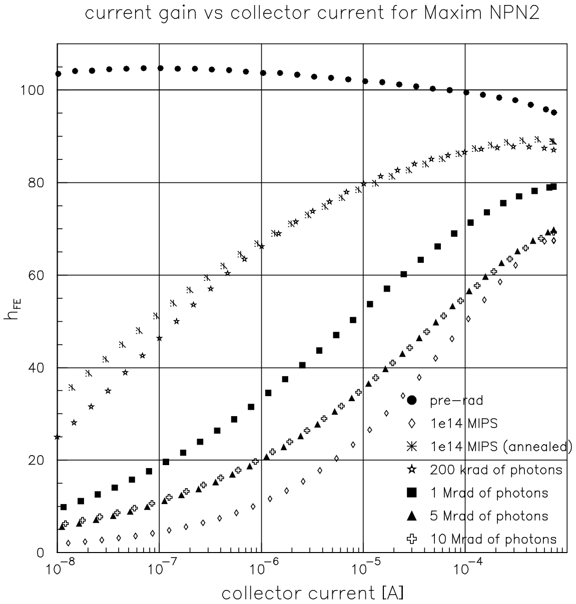

Figure 13-2 The current gain factor β vs collector current for the MAXIM CB2 process.

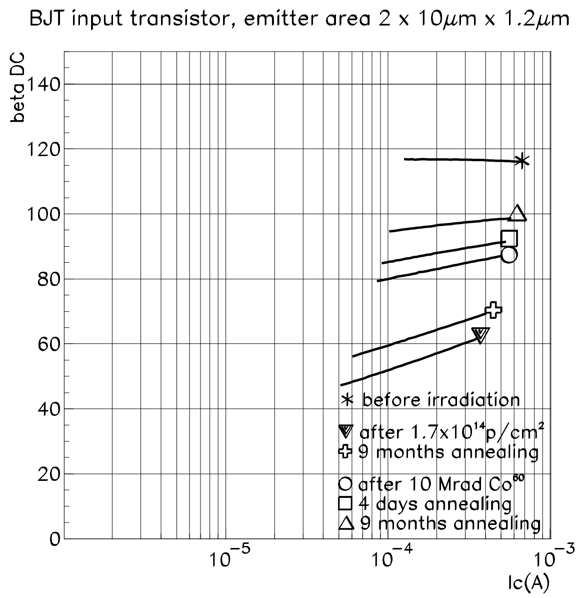

Figure 13-3 Summary of the effect of radiation on current gain for the DMILL bipolar transistors with the geometry used in the input front end transistor.

bipolar transistor. The DMILL transistors show in fact much lesser sensitivity to ionising radiation compared to the MAXIM transistors. For a minimum size transistor at a bias current of 100 μ A, after 100 kGy the β is reduced by 20% of the initial value while for a minimum geometry MAXIM transistor β is reduced by 50% after 100 kGy. The radiation hardness of DMILL bipolar transistors has been tested regularly by the technology vendor. Independently, different radiation tests have been performed by the SCT and Pixel communities with a special emphasis on transistors with geometry as used for the input device in the front end electronics. The summary of different radiation tests is shown in Figure 13-3 [13-2].

13.2.1.1 Effect on noise

For the preamplifier structures proposed for the ID, the noise performance and optimization of the bias current in the input stage depend on the absolute value of β of the input transistor. It is known that the radiation effect on β scales with the current density in the transistor and for the same absolute value of the collector current it is smaller for small transistors (higher current densities). The minimum size of the input transistor is limited by an acceptable base spread resistance which is a source of the voltage noise. Assuming that one keeps a constant collector current in the input transistor in order to keep the voltage noise low, a decrease of β due to radiation will cause an increase of the base current and the parallel

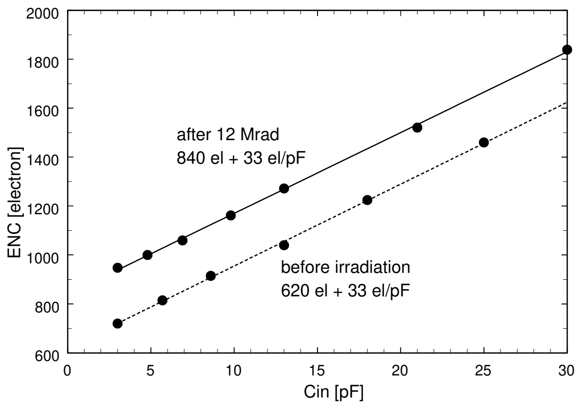

Figure 13-4 Noise as a function of the input load capacitance for the SCT preamplifier-shaper circuit realised in the DMILL technology.

current noise associated with it. This is an unavoidable effect at the device level but can be largely compensated at the design level. Figure 13-4 shows the plot of noise as a function of the input load capacitance for the SCT preamplifier-shaper circuit realised in the DMILL technology [13-2]. The increase of the parallel noise (for zero input capacitance) after irradiation up to 12 Mrad can be fully explained by a decrease of β and respectively an increase of the base current. For the extreme irradiation doses when the β may be reduced to a level about 40, one will need to reduce the collector current in order to avoid the noise being dominated by the parallel noise of the base current. Therefore, for the SCT preamplifier, the collector current in the input preamplifier transistor is controlled by an applied voltage. This is not necessary for the TRT preamplifier, because of the lower radiation dose and faster shaping time. For the Pixel preamplifier, control of the input bias current is being considered, although for other reasons.

13.2.2 MOS Transistors

For the SCT and TRT electronics, MOS transistors are employed mainly for the digital circuits. Therefore the analogue performance such as noise and transconductance behaviour with respect to radiation is not of primary concern for these systems. For the Pixel readout, preamplifiers using exclusively CMOS are being developed and measurements indicate that the noise performance is sufficiently good to doses exceeding 100 kGy. The main radiation effect relevant for digital circuits is the threshold voltage shift. For standard CMOS technologies the threshold voltage shifts are so big that they cause permanent failures of circuits after irradiation up to several hundred Gy. For the Pixel, SCT,and TRT systems, front end electronics radiation hardness up to 300, 100 and 50 kGy respectively is required and therefore radiation hardened CMOS processes must be used. Two excellent processes are the Honeywell 0.8 µm bulk CMOS process and the DMILL 0.8 µm BICMOS SIMOX process (Honeywell also has a CMOS SIMOX process which may be considered). The Honeywell process, like most available radiation hard CMOS processes, is officially *qualified* up to a total dose of 10 kGy. The use of the Honeywell process for ID front end electronics is based on the observation for a number of different rad-hard CMOS processes that radiation effects causing the threshold voltage shifts in MOS transistors saturate well below 10 kGy. Tests performed for the Honeywell transistors confirm this assumption and this process is expected to be sufficiently radiation hard for doses exceeding 100 kGy. It is important to note that the Honeywell process is triple metal, allowing very compact digital circuitry. It is also being used for rad-hard circuits by a number of other groups in high energy physics; both the SVX3 chip for CDF and the ADAM chip for BaBar are being produced in the Honeywell process. The DMILL process is *qualified* up to a level of 100 kGy.

The threshold voltage shifts after 100 kGy for typical small PMOS and NMOS transistors used in digital circuits for the Honeywell [13-3] and the DMILL [13-4] process are shown in Table 13-2. The numbers in Table 13-2 correspond to irradiation under typical bias condition.

Table 13-2 Threshold voltage shifts after 100 kGy for typical small PMOS and NMOS transistors used in digital circuits for the Honeywell and the DMILL process.

	Honeywell	DMILL
NMOS	-275 mV	-97 mV
PMOS	-275 mV	-180 mV

For CMOS circuits exposed to radiation, another effect to be considered is the probability of Single Event Upsets (SEU). Given the radiation environment of the ID, a certain rate of SEU will be observed. This is not dangerous for the operation of front end electronics as long as only soft errors in the digital circuits are caused by SEU. A SEU may in principle lead to latch-up which can cause permanent damage of the chip. The DMILL process, being a Silicon-on-Insulator process, is essentially latch-up free. While this is not technically the case for the Honeywell process which is a bulk process, precautions can be taken at the design level to increase the immunity of the chips to irradiation induced latch-up. SEU and radiation induced latch-up are strongly related to the designs and for chips in either CMOS, DMILL or another radiation-hard vendors, this aspect has to be tested extensively for the final prototypes. Initial tests on the SCT digital chip (CDP) implemented in the Honeywell process have shown no latchup, or other failure, after an exposure of greater than 250 kGy.

13.2.3 Production Strategy to Minimise Technical Risk and Cost

To minimise the risk and cost for the production of integrated circuits, ATLAS has established a policy that all rad-hard circuits should be prototyped in two radiation hard processes (unless good reason is shown why this cannot be done). As noted above, for Pixel, SCT, and TRT, the primary CMOS foundries being used are Honeywell and DMILL. For bipolar circuits, the primary foundries being used by ATLAS are Maxim and DMILL. The Harris bipolar and CMOS rad-hard circuits, the latter of which has been used extensively by CMS, provide still another alternative.

As discussed above in the individual sections, the Pixel, SCT, and TRT communities have prototyped at least the critical components of the required circuits in rad-hard processes. Full functionality “pre-production” chips are expected to be completed for the SCT by the end of 1997. For the Pixel and TRT systems, this is expected to be accomplished during 1998.

While it remains to perform radiation testing on much larger numbers of integrated circuits, ATLAS is confident that the required circuits can be delivered at a reasonable cost and in time to meet the schedule.

13.3 Grounding and Power Supplies

Given the very sensitive front end electronics in the inner detector, it is essential that stray electrical signals be reduced to a virtually negligible level, i.e., at least to the order of the thermal noise in the electronics. As discussed above, all signals in the Inner Detector will be transmitted either over fibre optics or via shielded twisted pairs. It is also essential to avoid any ground loops that could cause stray currents to flow near the sensitive preamplifiers.

To avoid ground loops, ATLAS has developed a policy that each subsystem will be isolated from earth except for the necessary safety connections, and isolated at least initially from the other subsystems.

While a number of details and final choices remain to be made, the following techniques will be used to isolate each system.

1. The mechanical mounting will insulate the TRT and the SCT/Pixel systems from the Liquid Argon cryostat and from one another.
2. All data and TTC signals will be transmitted over fibre optics or via low-level differential signals over shielded twisted pair. If the latter is utilised, the cable shield at one end will either be isolated from "ground" or connected via a capacitor to break ground loops at low frequency but allow optimum shielding at high frequencies.
3. LV Power Supplies - As discussed in the individual detector sections, a high modularity of power supplies will be used and the power supply returns will be isolated from ground, either via saturable isolation inductors, diodes, or no connection at all.
4. For HV distribution, the return or shield will be connected to ground at the power supply for reasons of safety, but will be isolated from the local detector "reference ground" by a suitably high impedance, e.g., resistor.
5. Environmental Monitoring - Signals from environmental sensors such as temperature monitors will either be received differentially or will be converted to digital format on the detector and sent via fibre optic or twisted pair links.
6. Cooling and Gas Distribution - Piping for services such as that used for distribution of the ionization gas, cooling gas, and cooling water will have short insulating sections to isolate the local piping at the detector.

Discussions have begun with the CERN safety contacts (see Section 16.5) to determine the optimal way to provide a safe system while minimizing ground loops over the widest frequency range possible. If saturable isolation inductors are required on the power supply returns at the power supply, then these would logically be the only connection to earth. If no connection of the low voltage power supply return to ground is required, as initial discussions have indicated is the case for voltages less than 50 V, then the local reference ground of the detector could be connected to earth. The system will be designed to allow considerable flexibility at the time of installation.

The installation of ATLAS detectors in the test beams provides an important test of the concepts to minimise noise. To date, the silicon and TRT detectors have been successfully operated at the desired thresholds.

Strict adherence to the principles above and tests of increasingly large assemblies of the detectors should lead to minimal noise in the final ATLAS configuration.

13.4 Off-Detector Readout Electronics

13.4.1 SCT and Pixel Readout Electronics

The SCT and Pixel detectors will have off-detector readout and control systems based upon components of common design. Each system will have its own DAQ LAN and TTC subsystem linking it to the ATLAS DAQ and TTC systems. These systems will interface to the 4088 SCT detector modules and the 2586 Pixel detector modules with approximately 11,000 40-80Mbps serial links total, and to the Trigger/DAQ system with approximately 400 1Gbps Readout Links. The SCT system will be housed in about sixteen data acquisition crates, and the Pixel system will be housed in about six crates. Each crate will contain a Readout Controller (ROC) and a

TTC Distribution Module. The ROC will provide local supervision of all readout and control operations in the crate. The distribution module will distribute TTC signals to Readout Driver (ROD) modules along a custom crate backplane based on differential strip lines. Other control, which originates in the ROC, will utilise a standard backplane and protocol. As many as sixteen to eighteen RODs will populate each crate. There will be 256 RODs in the SCT system and 81 in the Pixel system.

The SCT and Pixel readout and control systems will be operated by software executing within the Readout Controllers and Readout Drivers, and within the ATLAS data acquisition system. The software system will provide the code which controls the detector-mounted integrated circuits and the off-detector electronics, e.g. the code which will initialise, configure, and calibrate the electronics, diagnose electronics failures, and synchronise, control, and monitor the flow of event data. It will also provide the software framework for routines running within the Readout Controllers which will monitor the performance of the detectors, and it will provide all SCT and Pixel specific code that is required by the ATLAS data acquisition system for operation of the detectors.

13.4.1.1 SCT and pixel TTC subsystems and TTC distribution modules

Each SCT and Pixel readout and control crate will contain one TTC Distribution Module, which will receive TTC signals broadcast by the respective subsystem TTC transmitter provided by the Trigger/DAQ group. These signals will be received and decoded by custom opto-electronics and TTCrx receiver chips, also provided by the Trigger/DAQ group. The TTC Distribution Module will distribute the relevant subset of TTC signals along the crate backplane to the Readout Driver modules. The distributed signals will include the 40 MHz bunch crossing clock and a count of bunch crossings since reset, as well as the level 1 trigger accept and an event count. The TTC Distribution Module will provide a mechanism to optionally generate local TTC signals in order that a crate of readout and control electronics and its associated detector modules can operate in a standalone mode. It will also collect "buffer full" signals from RODs via the backplane and transmit them to the ATLAS level 1 trigger for trigger rate throttling.

13.4.1.2 Readout driver modules

The SCT and Pixel systems will use Readout Driver (ROD) modules of common design, with receiver sections, receiver protocol sections, and perhaps control output sections (see below) which are tailored to the specific needs of the SCT or Pixel system. The principal difference between the two systems is that the Pixel system anticipates that for the B-layer it will be necessary to deliver serial data streams to the RODs at 80Mbps, as compared to 40Mbps for the SCT. In addition, the data format for the two systems will not be identical, and the number of input data links per output control link may differ because of the different modularity of the detector systems.

For the SCT, each ROD module will service a group of approximately 16 detector modules by providing a serial stream of clock and control data and receiving two serial streams of detector data from each module. For the Pixels, each ROD will service a group of approximately 32 detector modules (arranged in 122 barrel ladders and 80 forward sectors) by providing two serial clock and control streams per ladder or sector and receiving one serial data stream per module. (Higher density designs servicing more detector modules per ROD are being investigated for both SCT and Pixel designs.) Close coupling of receiver functions and clock and control functions for groups of detector modules in the same Readout Driver will facilitate several of the synchronization and control tasks which will be performed by the ROD.

Receiver functions will be accomplished by five design blocks within the ROD:

1. **The receiver section** will receive input data streams on 32 serial links operating at 40Mbps coming from 16 SCT modules, or at 40-80Mbps coming from 32 Pixel modules. The input data may be any of three types: register data, calibration data, or event data.
2. **The receiver protocol section** will interpret the data protocol and check the data integrity of the incoming data on the asynchronous input streams. It will also synchronise the streams and multiplex and format the data. It will use time stamps and event id's received from the TTC System to properly associate event data from the different streams and to label the event records for subsequent event assembly. The Receiver Protocol Section will be the ROD's most complex design block. ASIC implementations of this block are being investigated in order to optimise cost.
3. **The monitor section** will separate calibration and register data (as opposed to event data) from the input data stream. It will also buffer input data, including event data, for access by the Readout Controller.
4. **The receiver output section** will transmit the event data stream via 1Gbps fibreoptic Readout Links to Readout Buffers in the Trigger/DAQ System. One Readout Link will be required for every 16 SCT or Pixel detector modules, resulting in one Readout Link per SCT ROD and two per Pixel ROD.
5. **The receiver control section** will control and coordinate operation of the various other functional blocks of the ROD.

Clock and control functions are accomplished by three additional design blocks within the ROD:

1. **The TTC input section** will receive ATLAS-wide clock and control signals from the TTC Distribution Module via the crate backplane.
2. **The control protocol section** will demultiplex commands broadcast by the TTC System and translate the TTC protocol into the SCT command protocol. It will then merge SCT-specific control commands into the command stream and direct the commands to the appropriate SCT detector module.
3. **The control output section** will output the clock and control in the common protocol on 16 control links (optical fibre or twisted pair) operating at 40Mbps, with one link per SCT detector module or two links per Pixel detector ladder or sector.

The Readout Driver is required to process instantaneous input data rates as high as 320 MBytes/s and to build event records at 75 kHz rates. The ROD is also required to distribute the ATLAS 40 MHz clock signal with a precision of 0.5 ns and to synchronise the trigger accept signal and the input data streams to one clock period. It is required to properly synchronise, assemble, and tag event data which arrive asynchronously on its input data streams. Finally, it must provide mechanisms to flag errors in input data and to throttle the trigger in order to avoid overflowing its buffers. We anticipate that the ROD design will be based upon gate arrays for the Receiver Protocol Section, field programmable gate arrays for most other logic, and a digital signal processor for control. In total, the SCT and Pixel readout and control systems will include approximately 256 RODs and 81 Pixel RODs.

13.4.1.3 Data acquisition software

Software will be a major component of the SCT and Pixel readout and control systems. Readout and control software must perform a number of critical functions in the distributed computing environment presented by the readout and control electronics. The principal software tasks of the readout and control systems will include:

- **Configuration**: Under centralised control, software will configure the off-detector readout and control electronics, and via the off-detector readout and control electronics, it will configure the detector-mounted readout ICs. Configuration includes such tasks as setting masks and downloading constants. It also includes more complex tasks, such as initializing the synchronization of data from all 4088 SCT detector modules and all 2586 Pixel modules.
- **Calibration and diagnostics:** Calibration procedures to measure electronics gain and noise will be executed under software control. Software procedures will also perform diagnostics of the readout IC's and diagnostics of the readout and control system itself.
- **Event data flow monitoring:** The synchronization of the flow of event data will be monitored continuously under software supervision. When an error is detected, software will resynchronise the electronics or report the error to higher levels in the readout and control or data acquisition systems. Error logs and statistics will be maintained.
- **Data quality monitoring:** Software will also monitor the quality of the event data as it is acquired. Samples of event data will be read from the Readout Drivers by the Readout Controllers. Quantities such as occupancy of strips will be histogrammed and filtered. Abnormal performance will be reported.
- **Standalone data acquisition:** Readout and control software will support operation of the SCT and the Pixels, or portions of these systems, independently of other ATLAS systems during commissioning and debugging periods. This capability will also permit operation of small data acquisition systems in laboratories and test beams during detector development.

Software tasks will be distributed over processors in Readout Drivers, Readout Controllers, SCT host workstations, and the ATLAS-wide Trigger/DAQ System. Many tasks will require concurrent processes on multiple processors. For instance, calibration procedures will involve code in the Readout Driver performing sequences of control operations on the readout IC's and compiling intermediate results of the calibration, code in the Readout Controller coordinating calibration activities in its crate and processing the calibration data, and code in host workstations supervising the procedure across crates and controlling voltage settings in the detector control systems.

The SCT and Pixel readout and control systems will be built upon a real-time operating system, such as LynxOS. The choice of the operating system will be made by the Trigger/DAQ group. The design of the readout and control software will include an overall framework which accommodates required software tasks. This framework will provide messaging systems necessary to coordinate tasks on different platforms. It will also provide interfaces necessary for specific routines, such as diagnostic procedures and detector monitoring. The SCT and Pixel software framework may be very similar to that of other ATLAS systems. Its design will be closely coordinated with the developers of the ATLAS Trigger/DAQ System.

13.4.1.4 Development plan

Over the past two to three years, readout and control electronics and software have been developed for use in laboratory and beam tests of silicon strip and pixel detectors and of readout ICs for both detector types. The test beam system performs several functions of the SCT and Pixel readout and control systems, although at a lower performance level. The central element is a DSP-based, custom VME card which performs functions analogous to those of the Readout Driver. The DSP card mates with custom low-level cards which interface to specific prototype versions of detector-mounted electronics. Software to control and read out detector modules and to communicate with the host VME processor has been provided. This system has been used to read out various prototype versions of SCT binary readout and of Pixel readout, and is currently being adapted to read out the prototype SCT ATLAS Binary Chip (ABC) and Pixel demonstrator module. It is now used widely throughout the ATLAS SCT and Pixel community.

As the first step in the design process of the production readout and control systems, an off-detector readout and control electronics requirements document has been drafted. This document itemises the functional and performance requirements upon the readout and control system in detail, and it will form the basis of the readout and control system specifications. In addition, for the purposes of estimating system cost, a preliminary cost model of the Readout Driver, including component count and board area estimates, has been developed.

The design and prototyping phase for the readout and control systems will extend approximately three years. Early in this period, a complete version of the readout and control system will be assembled using an early prototype of the Readout Driver module. The early prototype will concentrate development on the receiver, receiver protocol, and receiver output sections, with the purpose of demonstrating the required high performance of the readout protocol section. Two additional, full prototype readout and control systems are planned, the second serving as a preproduction model of the final system. Each prototype generation will include a new release of prototype TTC Distribution Modules, Readout Driver modules, and software, providing a full system test for all components. These prototype systems will be tested in laboratory and beam tests of SCT and Pixel detector modules, as well as on the bench. It is likely that they will also be incorporated into the prototyping efforts of the Trigger/DAQ group.

Custom electronics components (Readout Drivers, TTC Distribution Modules, and TTC backplanes) will be manufactured by industry and tested in house by ATLAS. A pilot run of approximately 5% of the production system will be manufactured and tested before release of full production. Standard components (crates, CPUs, and network) will be procured commercially. Software will be designed and coded in house.

Initial commissioning of the SCT readout and control system, starting with the first 5% of production, will occur at the site where modules are assembled onto their space frames. The system will then be moved to CERN, where final integration with the ATLAS Trigger/DAQ System will occur. Integration will be facilitated by the use of SCT readout and control prototypes in the prototype development of the Trigger/DAQ System.

13.4.2 TRT Readout Electronics

This section describes the required segmentation, functionality, and present development plans for the TRT system.

13.4.2.1 TRT readout segmentation

The data flows from the front-end readout boards to the Readout Drivers (ROD) and then to the Readout Buffers (ROB). This last element is common to all the Atlas sub-detectors and is used as data source by the Level-2 and Level-3 trigger systems. It is therefore very important that the data are stored in the ROBs according to the Regions of Interest (ROI) defined by the Level-1 trigger system. In the case of the TRT, a ROI is a $\Delta\varphi$ of $2\pi/32$. Therefore the readout has to be organised in subsets of this $\Delta\varphi$.

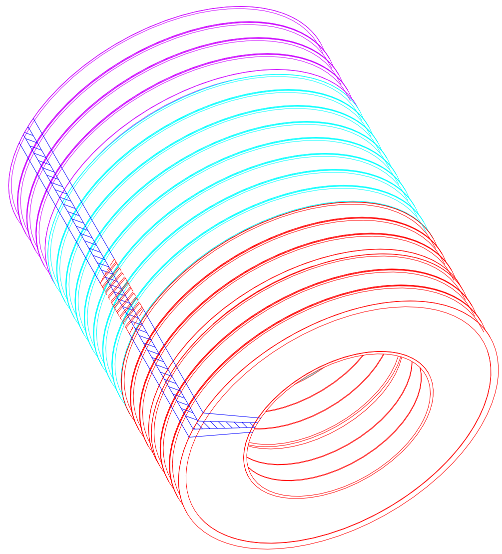

Figure 13-5 Readout segmentation in the End-Cap.

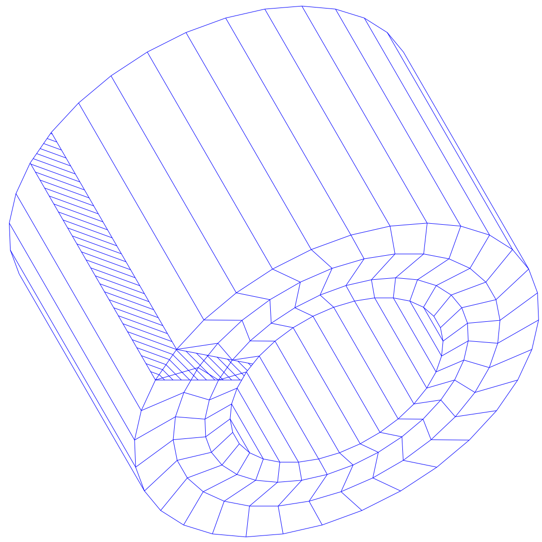

Figure 13-6 Readout segmentation in the Barrel.

Due to limited bandwidth and limited space in the RODs, the readout segmentation will be:

- **for the end-cap** 1/96 of each wheel. This leads to 128 straws in each wheel A, 64 straws in each wheel B, 96 straws in each wheel C and to a total of 1664 straws per ROD. As 16 straws are handled by each DTMROC chip, it means that a ROD reads out 104 DTMROCs. A trigger ROI will then be covered by 4 RODs and subsequently by 4 ROBs (including allowance for edge effects).
- **for the barrel** 1/32 of each barrel side is read out by one ROD. This also corresponds to 1664 straws or 104 DTMROCs. A trigger ROI will then be covered by 2 RODs and subsequently by 2 ROBs (including allowance for edge effects).

This gives a total of 128 RODs per side of the detector (256 for the overall TRT). In addition, the RODs which read out the end-cap and the barrel are identical. It is also important to note that the readout segmentation does not follow the mechanical segmentation (one ROD reads out a portion of 18 end-cap wheels) which has consequences for the timing and parameter control of the front-end: it is not possible to merge this part in a single ROD.

13.4.2.2 Data flow

Data flow is a very important parameter in the TRT due to the high occupancy of the detector. The expected input bandwidth of the ROBs which is 100 MBytes/s was used as an upper limit. This means that the link between a ROD and a ROB cannot exceed 800 Mbits/s.

For each L1A the ROCs transmit 27 bits (high threshold value :1 bit, low threshold value each 3 ns: 8 bits, for 3 consecutive beam crossings) of information per straw, plus control bits. This gives a total of 509 bits per ROC. A ROD receives data from 104 ROCs which gives about 52 kbits of information per L1A. Assuming a L1A rate of 75 kHz, this gives a total data rate of 4 Gbits/s which by far exceeds the 800 Mbits/s mentioned above. It is therefore necessary to implement in the ROD a zero-suppression scheme in order to reduce significantly the amount of data one has to handle.

Different zero-suppression schemes are currently being studied. For each of them, one uses simulated data for different luminosities (from 10^{33} to 10^{34} cm^{-2} s^{-2}) and includes a safety factor of two for the straw counting rate. The ROD design will allow changes of the zero suppression algorithm in order to adjust the amount of data exiting the ROD to the available ROB input bandwidth.

Although the fluctuations of the average event size are small, larger fluctuations from event to event due to the physics itself have to be accommodated. This requires an additional buffer in the ROD, acting as a derandomiser, before the transmission of the data to the ROB.

The zero-suppression scheme applies a gate of tunable position and width (see Section 3.7.5.2) to the data received from the front-end electronics. Straws with the low threshold bit set within this gate are considered as “valid”, and the information is reduced in the following way:

- For empty straws, only two consecutive bits set to 0 are transmitted.
- For “valid” straws, the complete information is transmitted (leading edges, trailing edge flag, high-threshold bit).
- For non “valid” straws which were not empty, only the low-threshold and high-threshold bits are transmitted.

Figure 13-7 presents for this zero suppression scheme, and for several different gate widths, the required bandwidth from the ROD to the ROB and the fraction of “valid” straws, as a function of luminosity. The event size distribution for a 25 nsec gate is also shown.

From these figures one can conclude that:

- The ROD-ROB link bandwidth is sufficient to read-out the TRT data even at twice the nominal luminosity.
- The event size fluctuations will be absorbed by the additional derandomising buffer of the ROD.

The large increase in number of “valid” straws when no gate is applied does not reflect in a similar increase of the ROD-ROB link bandwidth requirement since the event size is dominated by empty and non “valid” straws and since only a fraction of the additional “valid” straws have leading edge information to be transmitted.

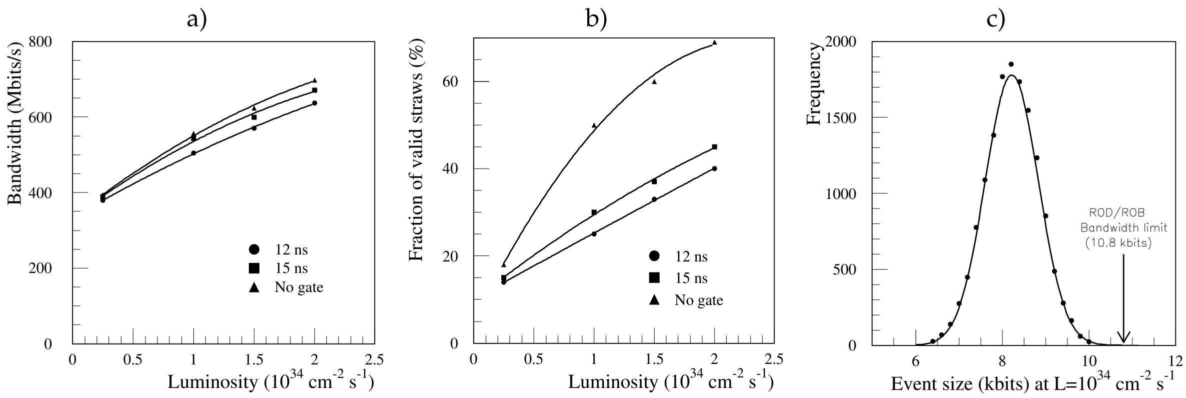

Figure 13-7 a) ROD-ROB bandwidth for a L1A rate of 75 kHz; b) Fraction of valid straws; c) Event size distribution at 1.5 10^{34} $cm^{-2}s^{-1}$ for a 25 ns gate.

13.4.2.3 Number of RODs for 100 kHz L1A rate

As noted above, it is planned to have one ROD reading out 104 ROCs. This segmentation will work for the maximum luminosity in the "descoped" version of the detector which assumes a L1A rate of 75 kHz. In the case of an upgrade of the detector such that a maximum L1A rate of 100 kHz must be handled, it is foreseen to upgrade the system by limiting the number of ROCs being read out by one ROD to 52. This would imply to multiply the number of RODs (and ROBs) by 2. The design of the ROD will be done in such a way that this operation is possible without a redesign and without losing the existing electronics.

13.4.2.4 TTC and parameter control

As mentioned above, the readout segmentation does not follow the mechanical segmentation of the detector. In particular, in the end-cap, a readout slice involves all the wheels. It is therefore impossible to have the same segmentation for the timing signal as for the readout as we need to adjust the BX timing at the level of the readout electronics with a precision of the order of 1 ns.

The timing and the parameter control signals will be distributed to subsets of 1/32 of each wheel and 1/32 of each barrel module. This granularity is small enough to avoid additional timing adjustments at the front-end level or complicated redundancy mechanisms for the distribution of the timing and parameter control signals (losing one of these connections means the possibility to lose 0.15 % of one detector side).

The signals that have to be distributed are the following:

- LHC Clock BX (timing signal)
- L1A signal (timing signal)
- Test_pulse (timing signal)
- Bunch Counter Reset BCR (timing signal)
- Event Counter Reset ECR (timing signal)
- Front-end Hard-Reset
- Address and data to write and read parameters (thresholds, masks,...)

In order to limit the number of cables that have to be installed in the detector, the protocol defined by the SCT community will be used:

- A single line is used to transmit the Clock, the L1A, the BCR, the ECR and the individually addressed data cycles. This requires the use of the DORIC chip at the front-end level. The test-pulse will be sent as a command on this line and only two different times are foreseen: one referenced to the rising edge of the clock and the other one to the falling edge of the clock.
- The readout of the front-end parameters is kept separated from the data readout (in contrary to what is foreseen for the SCT) in order for us to continuously monitor the front-end parameters.
- A separate line is used for the front-end Hard-Reset. This line could be removed, provided some other proven means (e.g. power off-on) exist to reset the front-end chips to a known state.

This leads to a total of 3 lines for the timing and parameter control of the front-end electronics.

13.4.2.5 System overview

Associated to the 96 RODs to read out one end-cap side and 32 RODs to read out one barrel side, one needs additional modules to distribute the timing and parameter control signals discussed in the previous section. This additional module is called the TRT-TTC and is discussed in detail in Section 13.4.2.7).

It is important to be able to partition the readout system for debugging, commissioning and calibration purposes. A total number of 4 partitions are foreseen: one per end-cap side and one per barrel side. We need therefore to have 4 TTC partitions provided by the T/DAQ system. This includes a TTC crate containing a TCCvi interface, a modulator, an optical driver and the optical fibres.

The back-end electronics will be housed in VME9U VIPA compliant crates located in USA15. Each crate will contain a VME master (not yet defined), 16 RODs and up to 4 TRT-TTC boards. A total number of 6 crates per end-cap side and 2 crates per barrel side will be necessary.

An overview of the system is shown in Figure 13-8.

13.4.2.6 Readout driver (ROD)

The main functionality of the ROD is to read out the front-end chips, to apply a zero-suppression algorithm to the data and to provide a formatted event block to a ROB through a readout link. In addition to that, the ROD includes tools for monitoring and debugging purposes. A block diagram of the ROD is given in Figure 13-9.

Readout block

As stated in the DTMROC section (12.8.3), data are transmitted from the DTMROC to the ROD serially at 40 Mbits/s. There is no protocol on this link and the system is based on the fact that the event size from one DTMROC has a fixed length and that the BX clock is used for the transmission. Nevertheless, the phase of the BX in the front-end is different from the phase of the BX in the ROD and it is necessary to make an alignment. For that purpose the DTMROC has the capability to transmit a succession of “0” and “1” pattern at the BX frequency. In the ROD, a TDC

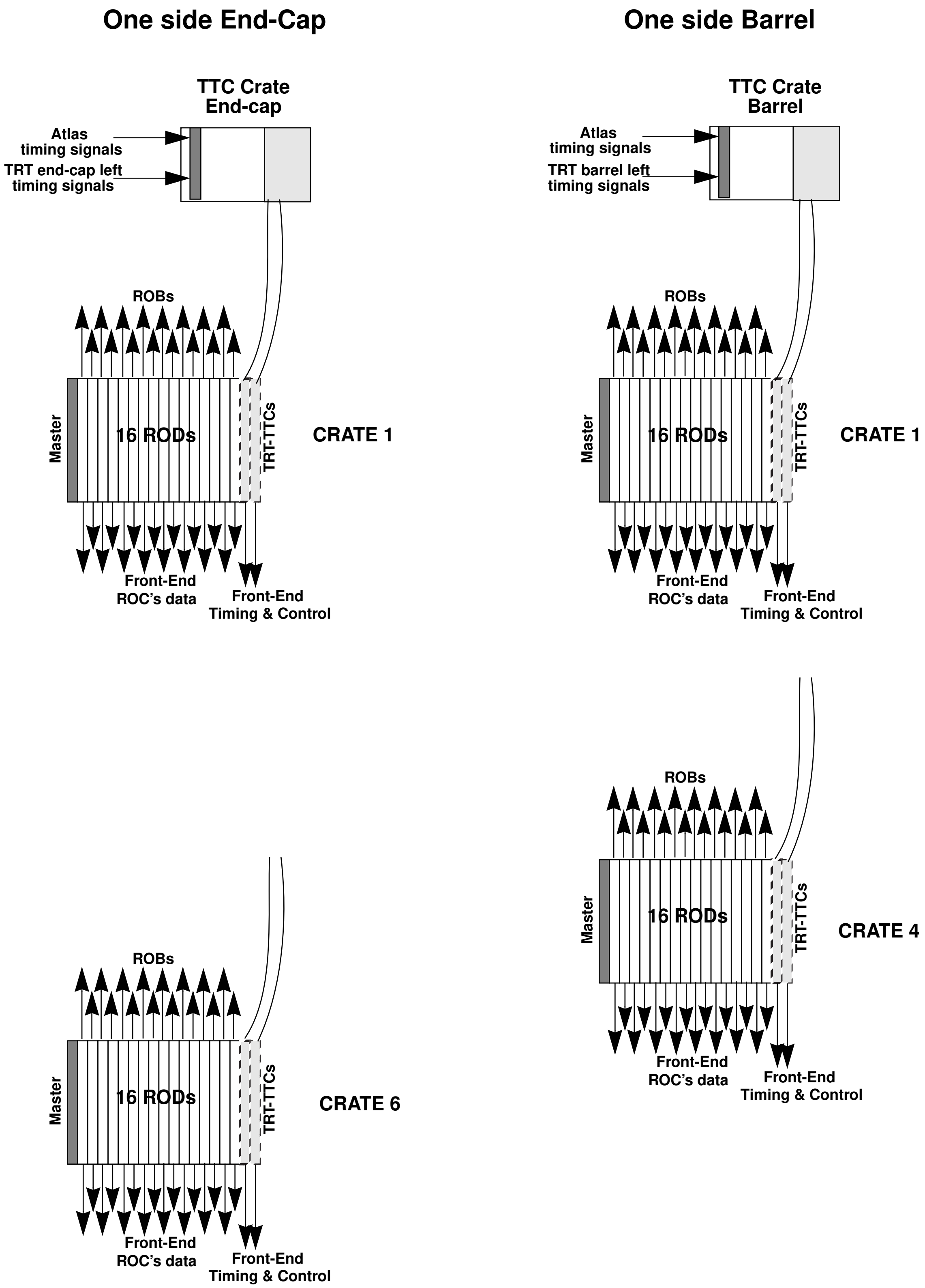

Figure 13-8 TRT system overview for one side of the detector.

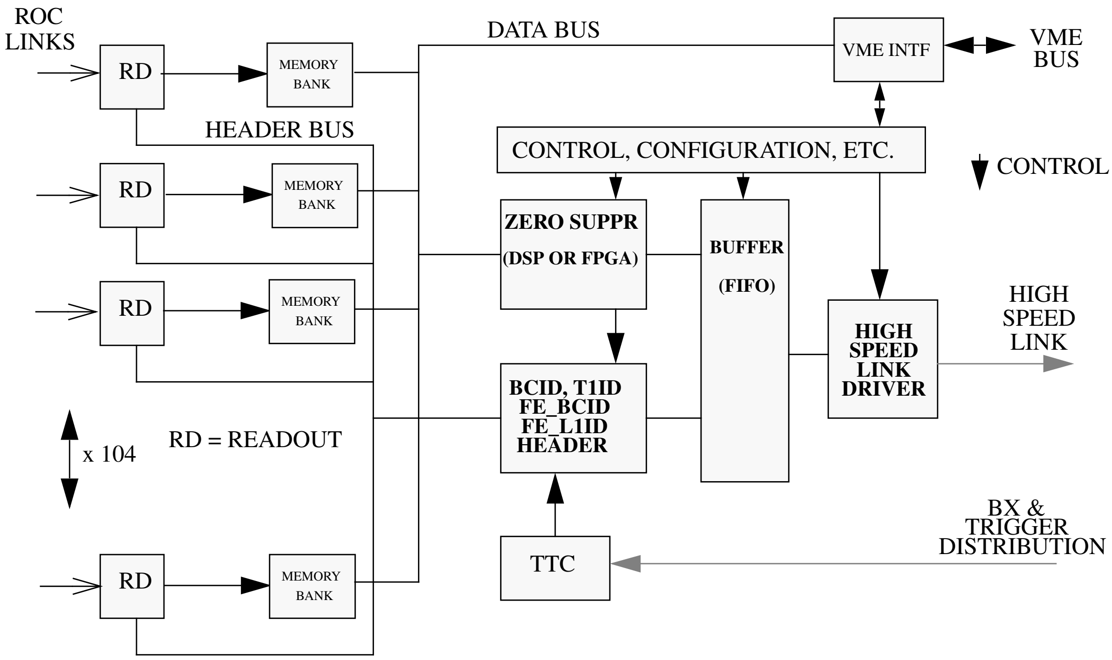

Figure 13-9 TRT ROD block diagram.

measures the phase of this signal with respect to the internal BX and depending on the result either the rising edge or the trailing edge of the internal BX is used to clock the incoming data. We benefit here from work done in the Level-1 Central Trigger Processor Demonstrator. The phase measurement requires a phase comparator followed by an ADC and a resolution of about 500 ps is obtained. Due to the stability of the relative phase of the BX used in the front-end with respect to the BX used in the ROD and the available margin at the input register (about 10 ns) it is not required to make this measurement more than once at the beginning of a run.

The data are then stored in a first buffer to allow coarse alignment between the different inputs. The header checker and the zero suppression circuitry use this buffer as data source. A VME accessible buffer is also foreseen at that stage in order to monitor the data before the zero-suppression is applied.

Header checker

Each DTMROC transmits a BCID number and a L1ID number with the data. In order to check that the readout electronics is still properly timed, the ROD checks that this information is the same for the 104 DTMROCs connected to it and that it is consistent with the BCID and L1ID received from the TTC system. If it is not, one of the status words of the event transmitted to the ROB will signal the error.

Zero-suppression

The zero-suppression algorithm will be implemented in reprogrammable FPGAs or Digital Signal Processors in order to be able to change the algorithm if necessary. At the output of that stage a full formatted event is built and stored in a FiFo before being sent to the ROB. If this buffer is full the ROD asserts a Busy signal which can be used by the Central Trigger Processor to reduce the L1A rate. The size of this buffer allows to store up to about 100 events which is large enough to absorb event size fluctuation.

In addition, the event is stored in a VME accessible buffer for monitoring purposes.

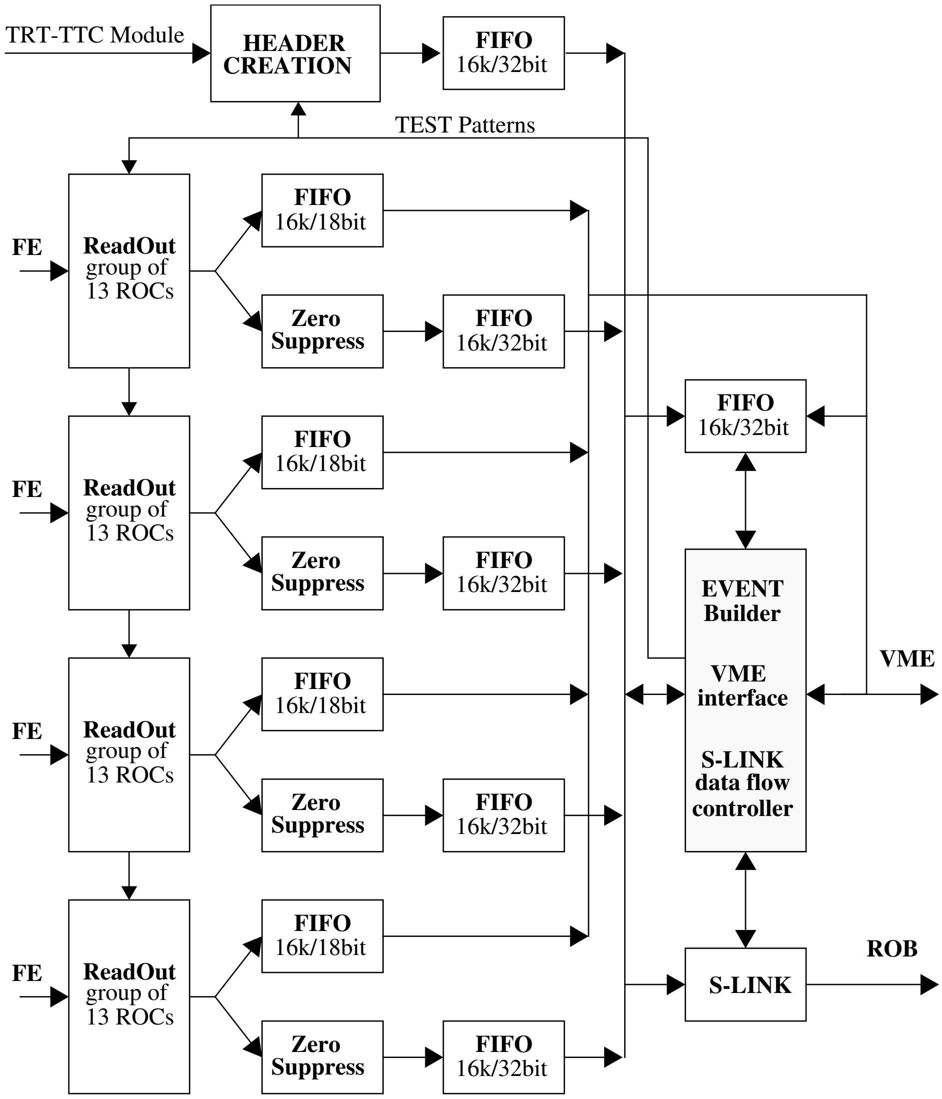

Figure 13-10 TRT Prototype ROD block diagram.

The zero-suppression and data formatting tasks will not introduce more than a few clock cycles of latency and will not introduced any dead-time.

Testing and monitoring facilities

As mentioned above, two monitoring buffers are implemented: one in which the non zero-suppressed data are stored and one in which the formatted data are store. A mechanism is foreseen to be able to monitor the same events before and after zero-suppression. This will allow one not only to check that the zero-suppression logic is working properly but also to monitor the loss of information that the zero-suppression scheme introduces.

This functionality also allows one to run the data acquisition without transmitting the data to the ROB. This is very useful for installation and debugging purposes.

The VME access to the monitoring data will be optimised in speed: both block transfers and chain block transfers (allowing to read out a full crate with a single DMA call) will be implemented and a readout speed of the order of 30 Mbytes/s will be achieved.

To be able to test the ROD without the front-end electronics, a test memory is implemented allowing one to simulate data coming from the front-end.

For production and maintenance it is foreseen to implement the JTAG boundary scan bus in this board.

TTC reception

The ROD needs to receive the BX clock, the L1A signal as well as the L1ID, the BCID and the Trigger Type. All these signals and data will be distributed by the TRT-TTC board through a custom backplane using LVDS electrical levels. The Busy signals of the ROD (warning that the output buffer is full) are transmitted to the TRT-TTC board through this backplane.

Prototype and production

A ROD prototype is being designed and should be used during the '97 test beam period (Figure 13-10). It implements all the functionalities described but for a limited number of inputs (52 instead of 104). The zero-suppression and data formatting logic are implemented in Altera FPGAs. The connection to the ROB is using the S-Link protocol.

After having validated the design of this ROD, the final version will be designed and the production will start in 2000 for a one year duration. The test of the production will be done after burn-in using first the JTAG internal facility (low speed test allowing to check the connections and components functionality) and then the in-situ testing capability at nominal speed.

13.4.2.7 TRT_TTC board

This board has two functions:

- It receives the TTC fibre, extracts the timing information and after proper delay adjustment transmits them to the front-end. In addition it provides the TTC information to the RODs of the crate through a dedicated backplane.
- It controls the parameter control link which allows one to read and write parameters and to transmit synchronous commands to the front-end.

The exact number of RODs associated with one TRT_TTC board has not yet been decided, but it will be of the order of 2 or 3 TRT_TTC boards per ROD crate. This leads to 12 to 18 TRT_TTC boards per end-cap and 8 to 12 TRT_TTC boards per barrel side. Each of the these boards will have to control 32 to 48 timing and parameter control links to the front-end.

As for the ROD, in-situ testing facilities as well as JTAG boundary scan bus will be implemented in this board to allow easy commissioning and maintenance. A block diagram of this board is given in Figure 13-11.

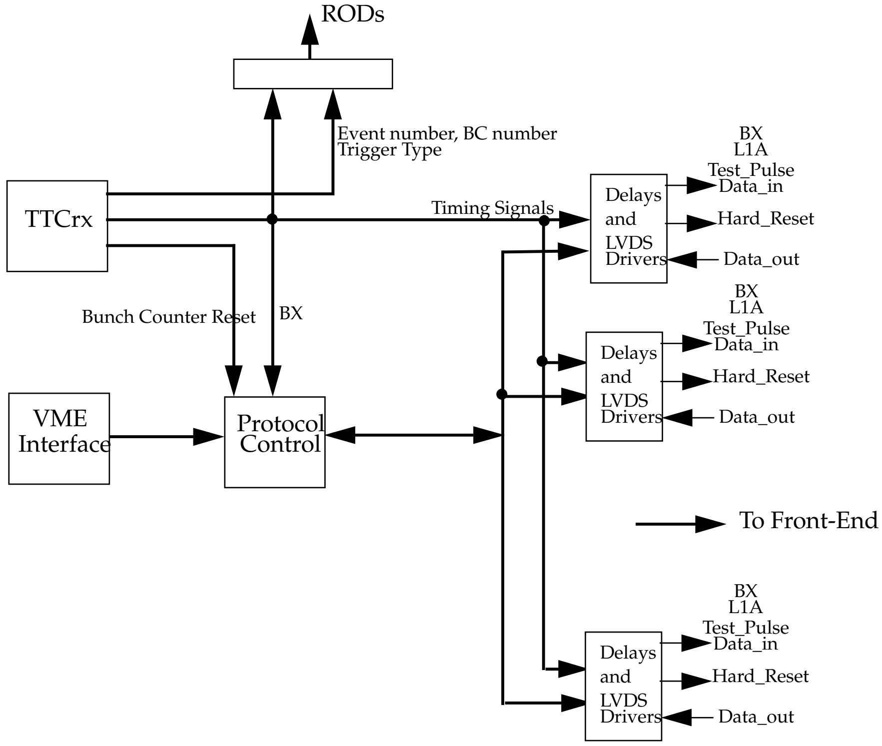

Figure 13-11 TRT-TTC Block Diagram.