11.10 Module Construction

This and Section 11.11 cover topics related to the fabrication of the tracker. The necessary activities are hierarchical and require careful staging. In the initial phase various components will be procured, tested and pre-assembled. Examples of these components are the detectors, front end chips, and hybrids which will be pre-assembled into modules. Other examples would include fabrication of DAT links, power tape bundles and cooling sub-systems from their vendor-supplied component parts. These activities will occur at many laboratories and institutes across the collaboration. In the latter phases, the tested sub-assemblies will be brought together at a smaller number of sites for final assembly of the tracker, as discussed further in Section 11.11. Clearly the staging of these activities is critical if the overall ATLAS construction milestones are to be met. In recognition of this, the SCT construction and assembly process is being designed and scheduled within the overall SCT project plan and managed by the SCT Steering Group.

11.10.1 General Considerations

Over an 18 month period leading to the publication of this TDR, the SCT group went through a series of internal design reviews which culminated in the selection of various baseline technologies to be used in the tracker. The development groups within the SCT have produced engineering specifications and designs for the various components. The construction programme must ensure that all these components are properly handled during assembly in an environment which will ensure good performance and long-term reliability of the tracker.

The first, most critical, and largest task in the construction sequence will be the assembly of the silicon detector modules. Since the SCT consists of distinct barrel and forward sections it is natural that module assembly divides along this boundary. Beyond this, in recognition of the large scale of the module assembly task, the SCT community is also divided into roughly geographical "clusters" each of which will work to test and assemble the module components. The clusters are described in more detail in Section 11.13. An important aspect of the module assembly process is ensuring that all modules are built the same way. To support this prerequisite, the community has adopted a set of working principles which are described below. In addition, the assembly process has been specified to be the same in all clusters.

The steps which follow module construction are covered in Section 11.11.

11.10.2 Module Construction

In this section a detailed description of the module construction process will be given. The SCT community is in a good position to accurately specify this process based on significant prototyping work and a broad background of experience coming from previous experiments. SCT collaborators have worked on silicon trackers for HERA, LEP and TeVatron experiments. The operational principles which have been adopted to ensure identical and reliable procedures in the various distributed construction clusters is presented first. A detailed description of the actual assembly process follows (Section 11.10.3).

While the module design process is aimed particularly at achieving certain performance specifications (noise, temperature gradients, etc.), it is clear that another set of issues exist which go beyond the module designate itself. Assembly procedures, quality control methods, production tests, application of adhesives are examples of items which impact more on the manufacturing aspect of this process than the physical choice of the module configuration. It is the purpose of the construction process design to focus on these issues of module manufacturing. A range of prototyping activities have been undertaken as part of defining the procedure. The result of this activity is as follows:

- module construction specifications have been adopted
- a set of working principles have been adopted
- the module assembly process flow has been specified
- a baseline mechanical assembly process has been designed in detail and partially prototyped. The costs and necessary infrastructure are understood.
- testing procedures have been specified
- production capacity and workload for the various sites/clusters has been specified
- technical issues for study and further prototyping have been identified

All these items will be described in additional detail below.

11.10.2.1 Aim

The aim of the module construction process is to supply the modules, including spares, for the barrel and forward SCT. The numbers are specified in Table 11-46. The schedule is specified in the project plan (Figure 11-122). Production is scheduled to begin in 1998, during which year at least some production modules will need to be delivered. It is therefore essential that some sites are functional by the middle of 1998.

11.10.2.2 Specifications

The precision needed during construction is determined by physics requirements. The overall requirements are listed in Table 11-33. The justification for these overall tolerances can be found in Section 11.8.2. The distribution of these allowed assembly tolerances between construction steps is not yet finalised, but only a small fraction will be assigned to module internal accuracies. As construction moves from the relatively small scale of module construction to overall detector assembly it becomes increasingly difficult to control mechanical tolerances. The precision available with modern mechanical fixturing and metrology is exploited in the module assembly to allow most of the available error to be assigned to the overall assembly steps. The module build tolerances follow below.

- Colinearity of strips on same-side detectors is required to be ±5 μm over their full length. This ensures negligible contribution to the r-ϕ measurement error.
- Wafer to wafer placement in z must be accurate to 25 μm. This limits the dead-space due to cracks between detectors whilst allowing reasonable ease of assembly.
- The overall position of the four wafers, considered as a rigid unit, along z, with respect to the dowel pin mounting holes should be within 100μm of nominal. This ensures uniform overlap of modules along z.
- Parallel translation of the ϕ strip centerline with respect to the dowel pin mounting holes should be within ±50 μm of nominal. This is required as part of the control over the overlap of modules in ϕ.

- The rotation of the module in the plane of the mounting surface is determined by the angle between the strips on the ϕ side and a line through the dowel pin mounting holes. The total allowed rotation (coming from trigger requirements) is 1.6 mrad. The contribution from the module construction alone should be less than 0.15 mrad.
- The stereo angle between sides must be 40±0.15 mrad. This accuracy eliminates the need for calibration constants for the stereo angle. A 0.15 mrad rotation results in a 10 μm shift in the position of the corner of the rotated wafer. Such a shift can be measured easily with the construction tools. This rotation results in a 240 μm systematic shift in the z coordinate measurement, small compared to the intrinsic resolution in z.
- The radial separation of the detectors as sandwiched must be constant to ±25 μm.
- If the dowel pin hole mounting surface and the detectors are not coplanar this will result in an error in the mounted modules tilt angle. The effect is small however since it goes with the cosine of this angle. Most of the concern then belongs to the integrity of glue lines and construction uniformity. Based upon this, the angle is specified to be less than 0.39 mrad. In this case the glue line thickness will vary by less than 25 μm.

11.10.2.3 Construction principles; working environment

This section defines the principals which the various module construction sites will adopt.

Unified construction procedure Each type of module for the SCT is expected to be identical (module barrel/forward) and to be constructed at multiple sites. The same construction process will be implemented at all sites in parallel. This is desirable for a number of reasons, in particular it is an effective way to maintain the same quality and uniformity across all sites. It also allows sites to benefit from each others experience. Finally, the use and fabrication of materials and fixtures may be optimized with the elimination of wasteful duplication.

A set of procedures and fixtures will be developed at one or more sites and then reproduced at all others. Multiple copies of precision fixturing will be machined at a single site for all users.

Centralized documentation The Rutherford Appleton Laboratory has been designated as the central repository for documentation. This includes indices, engineering drawings, material specifications, data sheets, material test results, samples, electronics documentation, procedure write--ups, test procedures, and QA documentation. It will be kept current and be available to all sites. Communication will be through a controlled process to ensure consistent updates of drawings and data.

Unified quality control process All sites must be kept to the same quality standard. Beyond agreed upon rules, a review process at each site involving members from the other sites will be employed. Strong lines of communication and personal familiarity of participants in the module construction process is important. In addition modules will be exchanged among sites for mechanical survey and test and for electrical test.

Centralized purchasing All materials used to produce modules, including disposables will be purchased centrally and then distributed to the production sites. This includes items such adhesives. By centralizing, the quality of the material used is controlled, ensuring that a bad batch does not contaminate the process at one site. In practice it will emerge that this approach is unnecessary in some cases. In those cases the item will be deleted from the central purchasing list at the time. But the basic default will be for all materials to be subject to centralized purchasing.

Production database A uniform database to track materials and modules has been selected. A prototype user interface has been designed. Data will be available to all sites. The chosen product offers significant flexibility in allowing the storage of unique and specific test results when needed. A typical user interface screen for the database is shown in Figure 11-100. More information can be found in a reference [11-90].

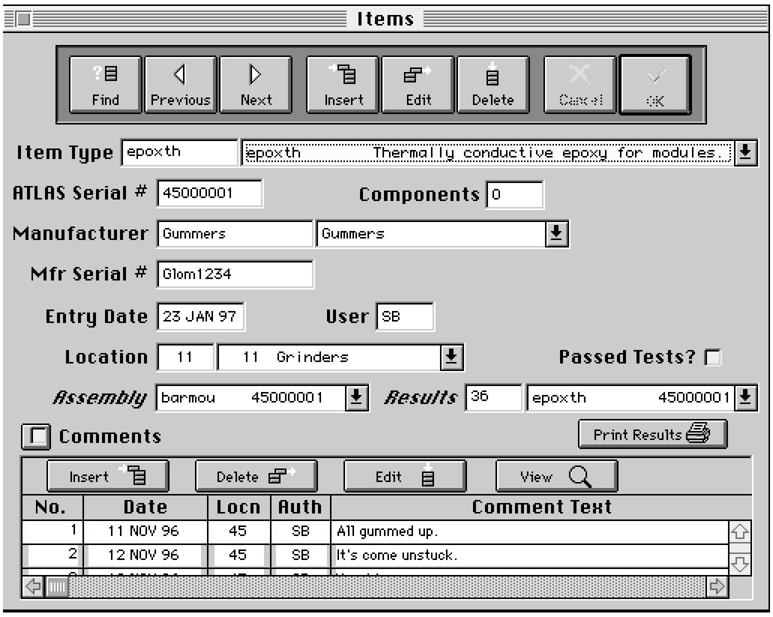


Figure 11-100 Database user interface screen.

11.10.3 Assembly Sequence

An overview of the assembly sequence is shown in Figure 11-101.

11.10.3.1 Component list

1. **Detectors** Each module consists of 4 single sided detectors.
2. **FEE** Each module contains 12 CAFE-M and 12 ABC (or 12 ABCD) chips. These chips will be fabricated in commercial IC foundries and be delivered to ATLAS-SCT in wafer form.
3. **Hybrids** Each barrel module contains two single sided thick film hybrids fabricated commercially on a BeO substrate. Each forward module consists of one double sided thick film hybrid fabricated on a BeO substrate.
4. **Cables/links/connectors** Each barrel module contains a short “pigtail” cable, a jumper cable from front to back, and an “opto-jumper” to make the redundancy connection to the next module. The forward modules lack the jumper cable. All these cables are fabricated commercially by a laminated copper on kapton “flex” cable process. Connectors will be purchased from a manufacturer. The optical components consist of DORIC and LDC chips, mounting hybrid, and fibres, all fabricated commercially.
5. **Misc. electrical components** This consists of various discrete components such as resistors and capacitors which will be purchased commercially in surface mount packages.
6. **Fan-ins** This thin film circuit will be manufactured commercially. Two are required per module with separate designs for the barrel and forward modules.

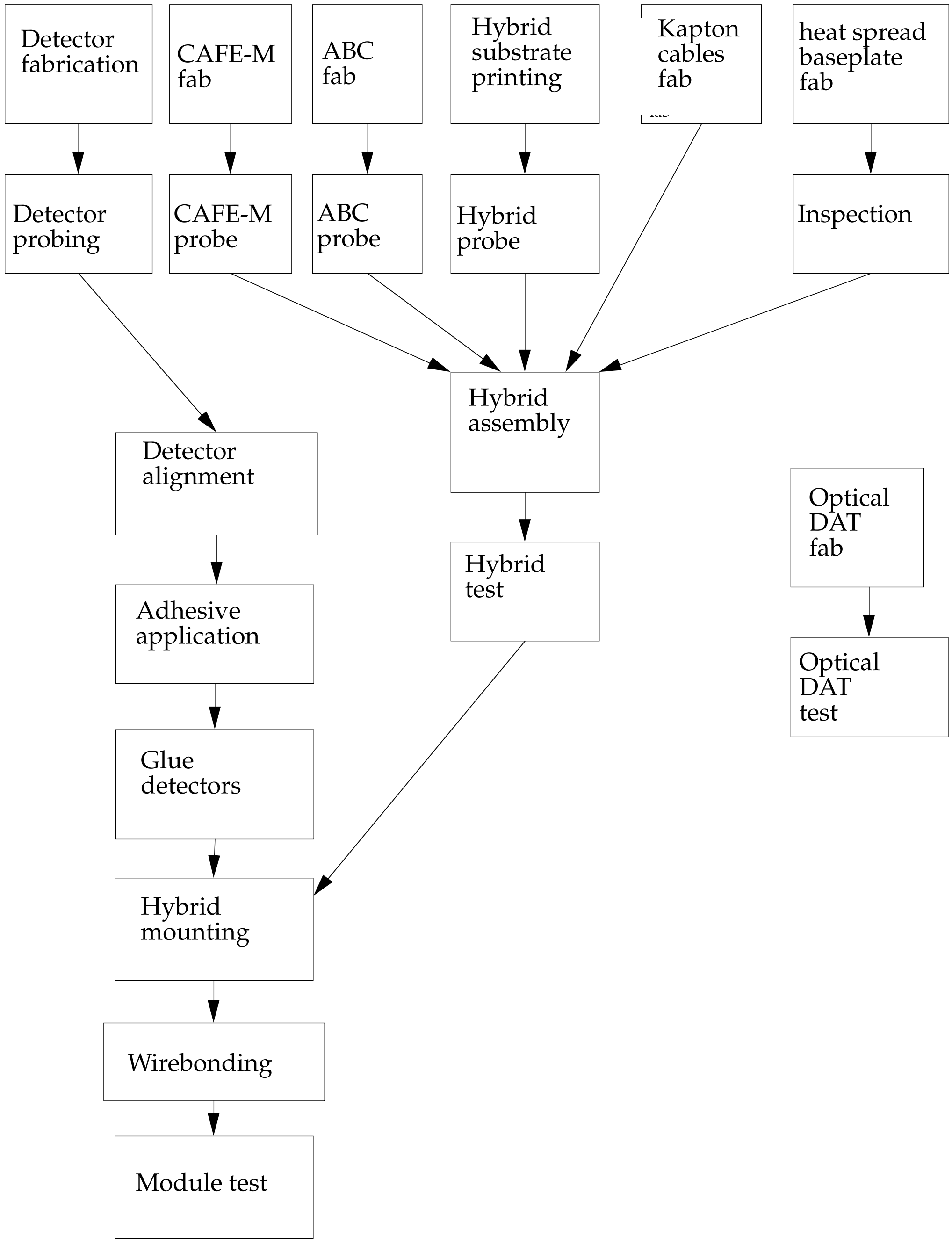


Figure 11-101 SCT module construction scheme.

7. **Thermo-mechanical elements** Each barrel module will contain two sheets of TPG base board which are purchased from the manufacturer. There will also be a BeO mounting plate, also fabricated commercially. The forward modules will contain only a BeO cooling and mounting spine, purchased commercially.

11.10.3.2 Test and inspection 1

This first set of tests and inspections is meant as a check on quality and performance of the procured parts. In some cases the tests will be performed by the manufacturer.

Test detectors

The manufacturers will be responsible for delivering detectors to the specifications described in Section 11.3.2 and for maintaining a stable process to ensure that the radiation hardness developed from the prototypes is continued during production. To determine if the detectors meet the specifications the manufacturers will measure, on all detectors, the IV characteristic between 0 and 200 V and the current of each strip to test for pinholes in the oxide. The latter will be measured at a specified applied bias. Further tests will be carried out by ATLAS institutes as described below. The results of the current-voltage curve and strip currents will be included in the data sheet supplied by the manufacturer for each detector.

After delivery all detectors will be re-inspected by measuring their IV characteristics, and any failing the specification on current at 150 V and 200 V will be rejected. If they pass the IV test, the strip currents and the strip capacitances will be measured. The strip capacitance is a test for shorts between strips, broken strips and broken connections between the implants and bias resistors. These measurements can be made in a single pass on an automatic probe station. If any detectors fail due to bad strips, they will be rejected.

Close contacts will be maintained with the manufacturer, and any significant levels of disagreement between the results of the manufacturers tests and those of the ATLAS institutes will be addressed.

Initially all detectors will be tested upon delivery. If the quality of the detectors is consistently good then the SCT project may require that only the IV curves be re-measured for every detector and the strip capacitance and strip current be measured only for a subset of detectors. For all devices, the SCT will require the manufacturer to perform their tests.

Additional tests will be carried out on a subset of 5% of the batch. The interstrip resistance will be measured between two strips near the edges of the detector and two strips in the middle of the detector. This gives information on depletion voltage, interstrip resistance and the bias resistance. To ensure that the detector performance is stable and will not change with the environment, 5% of the batch will be biased for a minimum of 24 hours in a N_2 atmosphere and their currents monitored continuously.

The standard test structure block will be provided and 5% will be tested from each batch. The following structures will be tested:

- Polysilicon resistor to monitor bias resistance,
- Large area diode to monitor depletion voltage and current characteristics,
- Aluminium resistance to monitor strip resistance,
- Metal implant capacitor to monitor coupling capacitance,
- Implant resistors to monitor implant resistance.

Detectors that are rejected will be returned to the manufacturer for replacement. If a large fraction of detectors or test structures are rejected then discussions will be opened with the manufacturers to evaluate the problem and possibly halt production until it is rectified.

The manufacturing process will be defined to optimise the radiation hardness of the detectors. To ensure that the radiation hardness is carried over into production a few detectors from batches of each manufacturer will be irradiated in the PS proton beam to 2×10^{14} pcm^{-2}. If detectors show increased radiation damage then discussions will be opened with the manufacturer to establish if changes have been made to the production process.

It is unlikely that every institute testing detectors will do so with identical equipment or start with the same experience. To ensure that the testing procedure is consistent across all centres, in the build-up to the production phase sets of detectors will be tested at several institutes. Cross-checks will also be made on pre-production detectors with manufacturers.

Test of front end chips

The development of tests for the front end chips will be the responsibility of the groups providing these circuits. Here details of the test procedures on production IC's are described.

The integrated circuits which will be part of the on-detector readout electronics will be fabricated by a commercial vendor. Before assembling these IC's onto hybrids they must be thoroughly tested to minimize the number of hybrids or modules that must be re-worked or discarded. Given that there will be upto 12 chip-sets on each module, any post assembly failure rate of IC's will quickly become prohibitively expensive. This chip testing also represents one of the largest uncertainties in the module production cost because IC test yields (the percentage of good chips) will vary from lot to lot due to fabrication process variations.

One of three chip test strategies will be adopted. The choice will be based on experience with production parts and be motivated by cost minimisation. Either

- The vendor will be paid to supply fully tested parts,
- Partially tested parts will be purchased,
- Untested, or minimally tested parts will be purchased.

The first is a strong candidate for the predominantly digital ABC. The third is a likely possibility for the CAFE-M with the mixed-mode ABCD likely to fall into the second category.

Price quotations were obtained for both tested and untested parts and a choice of strategy will be made in the light of future experience.

Whether tested or untested parts are purchased, ATLAS SCT must still have the equipment to fully test raw chips before assembly into hybrids. Some percentage of purchased parts must be evaluated even after complete vendor tests in order to audit the quality of the manufacturer's process and test procedures. In the case of testing exclusively to confirm quality, the percentage of parts tested will be adjusted during the production period based upon the results of the audit. Figure 11-102 shows a flow chart for IC testing . If tested parts are purchased then the first test box in the flow chart is actually performed by the vendor. If untested parts are purchased, all test boxes are performed by ATLAS collaborators in a self auditing fashion. The flow chart will apply for any of the possible production IC's, CAFE-M, ABC or ABCD. The details of the test itself will be different as described below.

A QA sampling test will be performed to validate the continued rad-hardness of the ICs from each fabrication lot. Again the sampling rate will be determined by the quality of the results. One or two dice per wafer is a likely starting level of sampling. These dice will need to be mounted on test boards and tested before and after irradiations.

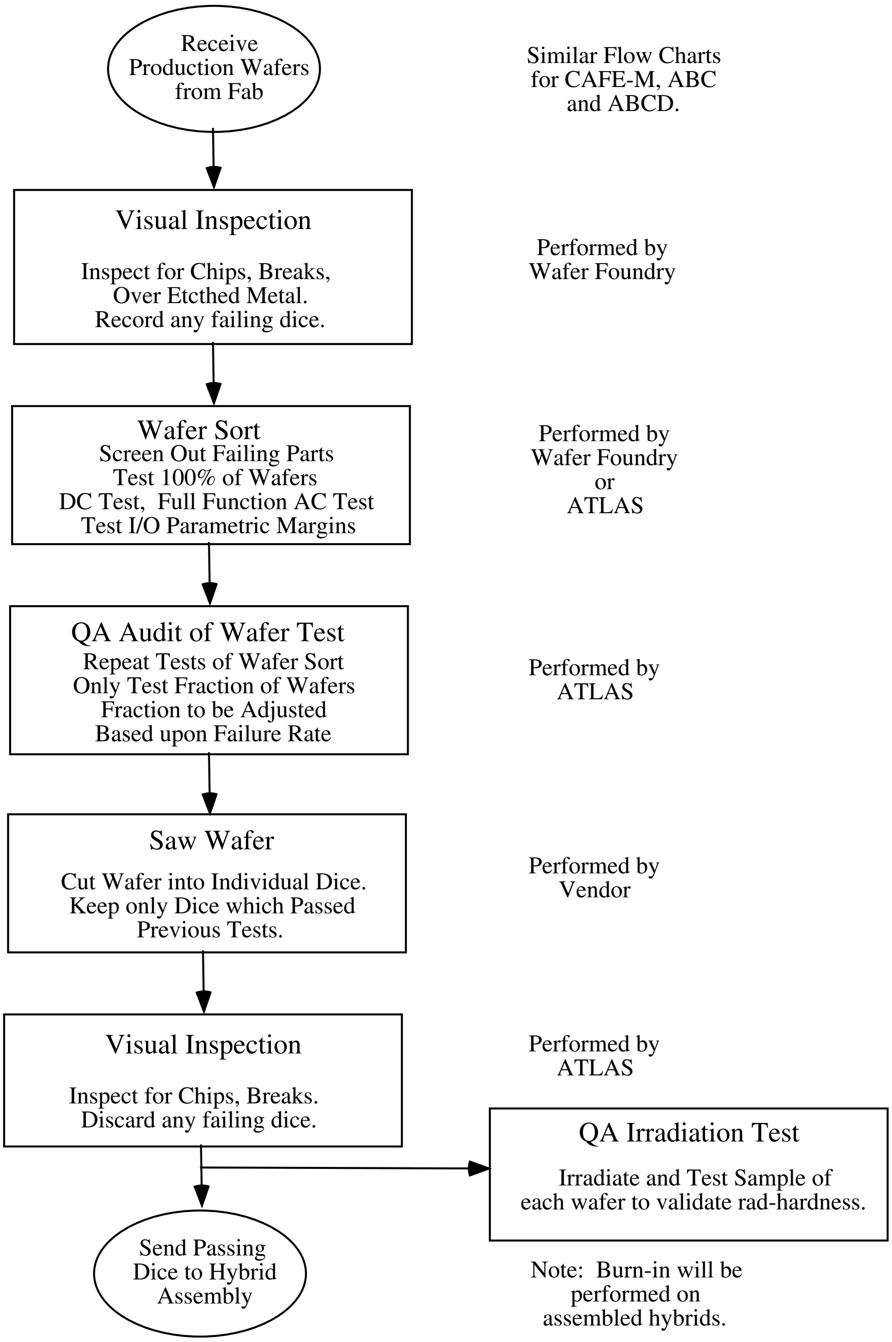


Figure 11-102 Flow chart of IC testing procedures.

Electronics, and ICs in particular, suffer from infant mortality. Operation for a period of ~100 hours after packaging is standard industry practice. SCT front-end ICs are not packaged. Burn-in as part of a wafer test would be too expensive. Burn-in after assembly to the hybrids will be time consuming and rework of hybrids to replaced failed ICs might compromise their long-term reliability. The burn-in strategy requires more study during the final year of prototype evaluation. The amount of burn-in required and the failure rates will be established by studying prototype and pre-production parts from the selected vendors.

Details of wafer testing

Depending upon which vendors are finally chosen for IC procurement, testing may have to be done on an analogue bipolar IC, a digital CMOS IC or a mixed signal biCMOS IC. From the standpoint of test engineering, the third possibility presents a merging of the other two requirements with some simplification possible. The first two possibilities will be discussed first and then the similarities and differences as applied to the biCMOS case highlighted.

CAFE-M testing This chip has 128 independent channels which must be tested as well as some common support circuits. The pad density is such that probing all 128 channels simultaneously will be difficult if not impossible. It will be possible to avoid probing the input pads since the internal calibration circuitry (see Section 11.4.4.1) can be used to inject charge into each channel just after in the input bond pad. Testing via calibration pulses will provide excellent fault detection since only the pad itself and a very short metal trace will not be tested. However, all 128 output pads must be probed in order to validate that each channel is functioning. A scheme has been developed by which one probe card probes half of the 128 channels but can be used in two successive positions on the die. Thus all 128 channels can be checked in two steps. This will reduce the number of probe contacts by two and make the testing feasible in an affordable amount of time. To probe all the necessary pads, a membrane style probe card will be employed. This should also provide a better noise environment for making the necessary analogue measurements.

Since the input and output of this IC are not standard digital signals, special interface circuits have been designed to transform digital control signals and to measure the amplitude of the output signals. These circuits will be interfaced to standard data acquisition modules which are used to control the testing and log results via a computer.

- The test sequence will start by applying DC power to the IC and measuring relevant currents. These will include the main current draw of the IC and the currents drawn by the reference circuits. To pass, parts must have current readings within specified limits.
- Next a calibration pulse of variable amplitude will be applied for several comparator thresholds. In this manner, the full response range of the circuit will be measured.
- Since the calibration circuitry relies upon signals externally controlled, but internally generated, an externally generated charge will be injected into a few channels to cross-check the accuracy of the calibration circuitry.
- The quality of output signal will be measured: passing parts must produce a “hit” signal above a minimum level and a “no-hit” signal below a minimum level.

DC and AC tests will be performed at minimum and maximum voltages. AC tests will be performed with control pulses at nominal speeds. Wafer testing will be performed at room temperature. Since the parts are expected to operate between -10 ^{o}C and 30 ^{o}C, no high temperature testing need be performed. Cold testing at wafer probe is very difficult and costly so test performance will be extrapolated to cold temperature and then validated with assembled hybrids.

ABC testing As with CAFE-M testing, all the 128 input pads need not be probed since the ABC has internal test circuits to inject signals into each channel and to vary the amplitude of the injected signal. The output pads present less of a problem in this case since the outputs from all 128 channels are serialized. Therefore, a standard probe card can be used to test the ABC.

While the internal circuitry of the ABC is predominantly digital, many of the inputs and outputs are not standard digital (i.e. CMOS) levels. There are current drivers or limited swing voltage receivers. For this reason a special interface card has been designed to translate these signals into standard digital signals for the pattern generator and analyser. This interface card also provides the capability to vary the amplitude of the input signals and measure the amplitude of the output signals. This allows for full parametric measurements of the inputs and outputs. This is necessary to ensure that the ICs work over the required ranges and will interface properly to the other circuits in the readout system.

The test sequence will be driven by a programmable pattern generator and responses captured by an buffered input register. The current design of these are VME modules interfaced to a computer. If available, a commercial high speed tester could be employed.

- The main test sequence will consist of inputting various data patterns, propagating them through the pipeline and reading them out. Each of the different input, data compression and output modes will be tested.
- In addition, each of the possible error conditions will be tested (such as receipt of token with no event pending or overflow conditions after too many consecutive events).

Tests will be run at minimum and maximum voltage and full 40 MHz speed. Wafer probe will be run at room temperature with expected performance extrapolated to -10 degrees.

ABCD testing This IC incorporates all the circuitry of the CAFE-M and the ABC. The test sequence will therefore, be the sum of the test sequences of the two other ICs. However, since the outputs of the ABCD comparators are not brought to output pads but rather are fed directly to the equivalent of the inputs of the ABC IC, there is no need to probe the output of the channels directly. The calibration amplitude and the threshold can be varied by commanding the internal controls. The response of the comparators can be measured by allowing the signals to propagate through the pipeline and be serialized at the output. The general sequence will be to first perform a DC test, then perform an AC test on all the digital circuitry and then use that digital circuitry to test the analogue circuits.

Full parametric testing As described above, full parametric test capability will be available for all the ICs. Ideally, a minimum and maximum acceptable limit will be established for each parameter to guarantee performance over the necessary operating conditions and with proper interface to the other circuits in the readout system and with some guard band for tester inaccuracies. However, if it is found that the spread of manufactured parts is so wide that the yield to such a min/max test is low, it will be possible to place parts into one of several bins according to their parametric responses and then match parts. This technique increases test time and makes material control more difficult, but will be employed if required to increase yield and lower costs.

Test fan-ins

The fan-ins connect the pre-amps to the detectors. These are thin film circuits on ceramic. All lines must be continuous with no shorts between neighbouring lines. Either the fan-ins will be probed on an IC station or they will be optically inspected, possibly using a pattern recognition system. Opens can be repaired by wire bonding. Shorts can be scraped open with a probe needle and manipulator. On a “lot” basis, fan-ins will be tested for wire bonding compatibility by being attached to hybrids.

Test cables

The short flexible cables will be tested by the manufacturer and spot checked by the construction groups.

Optoelectronic testing

The optoelectronics consists of the LDC and DORIC chips, the LED/PIN package and passive components. Strictly this is parenthetic in this section as the optoelectronics is not part of a module.

- The optoelectronic package will be tested by the manufacturer. These tests will involve measurement of the launched power of the LEDs and the responsivity of the PIN diodes.
- Functionality of the LEDs and PIN will be checked after a burn-in period by the SCT community.
- The LDC chips will be fully tested by the SCT community at the wafer level using a conventional probe card and probe station. Full speed tests will be performed on a sample of chips from each wafer, bonded out to a test card for this purpose. These chips will also be irradiated to confirm the radiation hardness of the fabrication run.
- Simple functionality tests will be done on a similar type of probe card for the DORIC chip. As for the LDC a sample of the chips will be bonded to test cards, run at full speed and irradiated.

Burn-in procedure will be developed, as for the other front-end chips, on the basis of prototype and early production chips. The chips and optics will be tested over the full temperature and voltage range required.

Inspection of mechanical components

Mechanical components include the TPG insert and the BeO mounting piece. Mechanical inspection will consist of dimensional measurements and optical inspection for defects. If thermal conductivity proves variable, "lots" may be measured for this property.

Test unloaded hybrids

The unloaded hybrids must be checked for continuity and shorts. Since there will be of order 100 nodes on a hybrid they will be probed automatically. A two probe "flying probe" system is well suited for this. These tests will be done by the manufacturer.

11.10.3.3 Pre-assembly

The next set of steps consist of various pre-assemblies which proceed the actual module construction. The most substantial result of this phase is the assembly of the electrically ready hybrids.

Dice wafers Once chip testing is complete the wafers will be diced with a wafer dicing saw. Dimension controls will be specified to ensure proper mounting on the hybrids.

Parts kit formation Based upon the results of parametric tests some sorting of die and also discrete components may occur. The analysis codes which process test data will be written to drive this process in an efficient way.

Optoelectronics assembly The DORIC and LDC chips are glued to the ceramic chip support part of the opto-electronic package. The LDC, DORIC, LEDs and PIN diode are then wire bonded. The 2 capacitors and connectors are mounted on the ceramic opto-hybrid. The opto-electronic package is then glued to the opto-hybrid.

Assemble hybrids Hybrid assembly consists of part mounting and wirebonding. The parts mounting steps, consisting of soldering of cables and surface mount components and gluing of chips and fan-ins can be done commercially or within some SCT construction groups. The wire-bonding steps, requiring non-standard high density bonding and strict quality control, will be done by SCT construction groups.

11.10.3.4 Test and inspections 2

This set of tests and inspections is aimed at assuring the quality of the assembled hybrids and optics.

Test hybrids These tests are based upon the tests of the FE electronics. They will include threshold, occupancy, noise, and gain measurements on completed hybrids.

Rework hybrids Some hybrid failures may be traceable to components on the hybrid, in particular FE chips which failed some time after wafer probing. In principle FE chips can be removed and rebonded although the ultimate effect upon reliability will have to be assessed carefully. In the case of rework, strict procedures will be adopted so that the final hybrid is not somehow compromised by the repair process. Rework will follow a well documented decision process and be recorded in the database.

Encapsulation Subject to confirmation of radiation tolerance, tested hybrids will have their wirebonds encapsulated. Removable encapsulants have been used in the past with success.

Retest hybrids Hybrids will be fully retested after rework or encapsulation.

Burn-in hybrids This step is meant to eliminate early failures. Typical burn-in schedules call for 100 hours at raised temperature. Fixtures will be prepared to allow efficient burn-in of many hybrids in parallel.

Test of opto-electronics The following tests are performed on the complete opto-electronic package. The details of these will evolve as prototype systems become available.

- BiPhase mark data is sent to DORIC from an SCT-TTC module. The recovered clock signal is examined on a digital oscilloscope. The input mark/space ratio and light fall and rise times are adjusted and the lock-in range confirmed as being consistent with specifications.
- A fixed pattern of data is sent to the DORIC from the SCT-TTC and the output data is compared with the input data by reading it into a ROD.
- The LED fibres are connected to a ROD. An LVDS driver is used to send data to the LDCs and the recovered data is checked to be correct over the operating current ranges.

Parts kits formation Hybrids and detector crystals may be grouped together into modules based upon some optimization criteria (bad strip overlap, uniformity, etc). The selection will be made with an appropriate software filter to ensure a documented procedure and outcome. This will be driven by the construction database software.

11.10.3.5 Module mechanical assembly

The technical requirements on the precision of the module assembly procedure were described in Section 11.10.2.2.

The assembly procedure is undertaken in three distinct phases. Initially, all the component parts are inspected and their serial numbers checked against those in the construction database. In this way, all components can be traced from manufacturer to completed module operating inside ATLAS. The second element of the construction program concerns the positioning of the four silicon wafers onto a beryllia baseboard. In this baseboard are the precision reference holes that will determine the final location of the module on the local support, and hence within ATLAS. This stage of the construction will be automated since this offers the benefit of constructing near-identical modules at a number of remote sites. It eliminates the need for human alignment of 80 μm pitch diodes on two pairs of detectors, which is potentially the most labour intensive and tedious phase. The system chosen will perform this repetitive alignment task, always to the same precision. Provided that identical software and compatible hardware is used at all assembly sites, the modules produced will be free of local identity.

The third part of the construction process involves attaching the hybrids to the modules. This is achieved with purpose-built, precise jigs that can all be manufactured at the same location or machined to the same set of CAD/CAM instructions. Again, this approach will benefit the experiment, leading to greater consistency and offer the freedom to position modules on local supports without a knowledge of their production site.

Figure 11-103 depicts a schematic of the proposed system of SCT module assembly with all the major components shown. The technique relies upon the use of a fixed camera to provide the reference point from which all computations are made. The various module components can be moved underneath the camera using a mixture of linear and rotational stages. Once aligned, two detectors would be transferred to another vacuum chuck (transfer platen TP1 or TP2; see Figure 11-105). Two such platens, each holding a pair of pre-aligned detectors, are themselves aligned with linear bearings and high precision shafts.

The main assembly station consists of two large, orthogonally mounted linear stages. on top of these are mounted two stacks of 'x', 'y' and 'rotate' stages. On top of these are held two vacuum chucks, upon which the p-side (back-side) of the silicon detectors are held. In order to give the operator maximum access the stages have been arranged such that their motors and cables are mounted at the side and rear when viewed from the operator's standpoint.

A structurally strong, vertical wall, housing two linear bearings, is fixed in front of the stages. One bearing is an adjustable diameter, steel item which defines the XY position while the other is a fixed, plastic version defining the rotation. Since the position of the bearings and the pillars in the transfer platens cannot be absolutely correct, a small degree of flexibility is thus achieved. By placing the bearings in the wall rather than the platens a very sturdy assembly is constructed, with the additional benefit that the transfer platens which will pick up the aligned detectors can now be relatively thin, since they are carrying the fixed pillars. The use of only two bearings has the attraction of further minimising the overall dimensions of the transfer platens (TP1,TP2). With the pillars mounted in the platens, the entire item may be easily exchanged if damaged. Initial setting up of the equipment will ensure that the line between the centres of the bearings is in the same plane as the camera. The rotation of 40 mrad between the stereo and "r-ϕ" sides is achieved by an offset in the bearing position in TP3 which has the advantage that neither the operator nor the software has to monitor that aspect of the module construction. The design of the third transfer platen (TP3), is such that it provides protection in the handling of modules during the later stages of production.

The alignment of each detector pair is achieved using fiducials produced on the metal layer of the processed silicon detector during manufacture. Since this processing is an inherent part of the detector manufacture, the internal alignment of the diodes to the fiducials can be guaran-

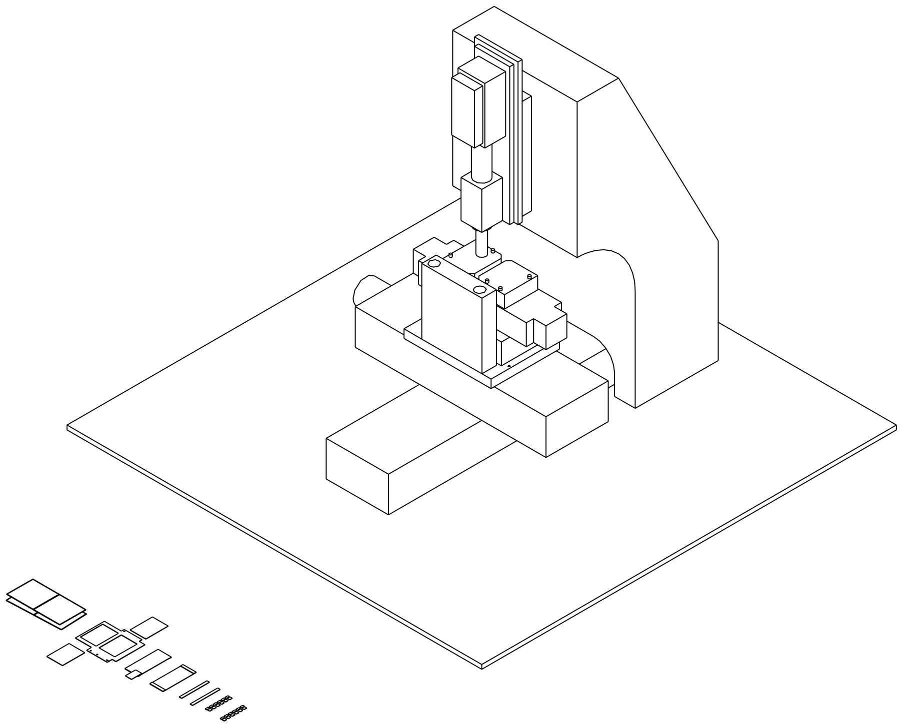


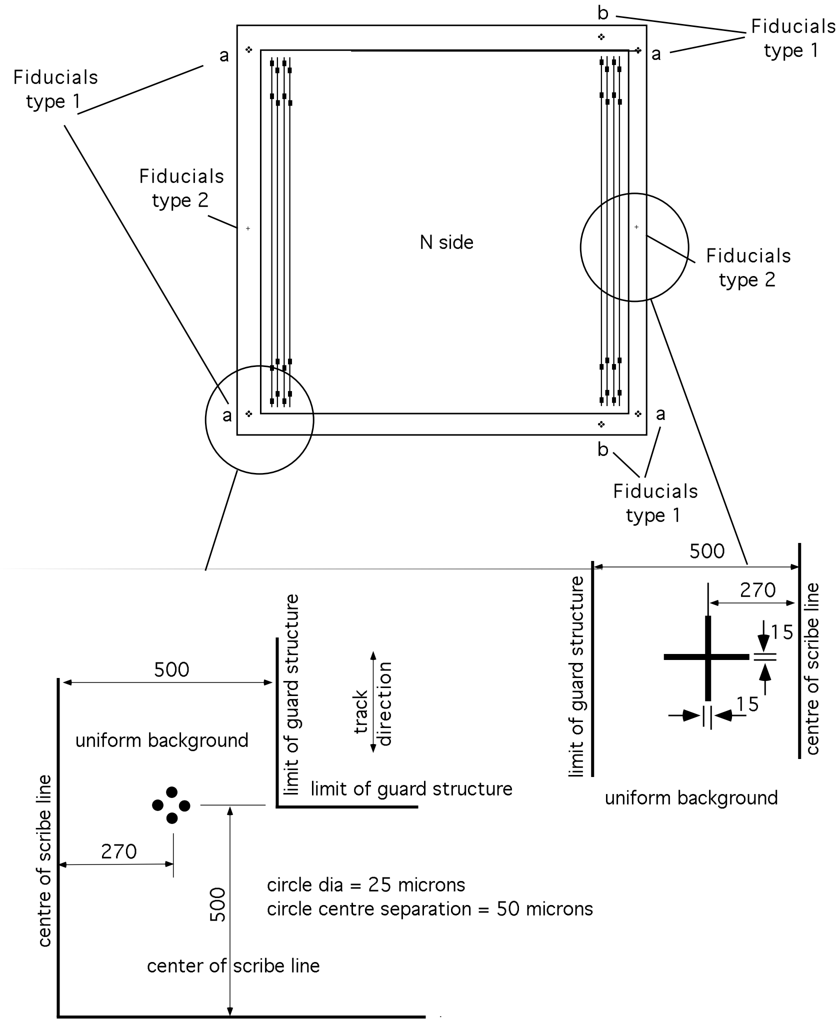
Figure 11-103 The SCT module assembly station with module components.

teed to the level of the manufacturers quality control. (Typical mask to mask alignment errors are of the order of 2 μm).

In order to simplify the task of the pattern recognition software a specific fiducial was designed. These fiducials are required for automatic alignment of detectors using digitised images received from the alignment system camera. Each fiducial takes the form of 4 circular dots of 25 μm diameter, grouped to form a square pattern, as shown in Figure 11-104. The advantage of a round dot is that it is insensitive to rotation of the detector. This allows the software to construct a bounding box with well defined dimensions around each dot. The centre of the array of the 4 bounding boxes can then be computed. This gives a centre for the whole array with inherent redundancy, since only three of the four dots are required to formulate this centre.

Since the design of the detectors means that they are not quadrant symmetric, they must be placed in a specific relationship to each other to form a pair. The fiducials marked (b) provide this asymmetry check, whilst those fiducials marked (a) are used for alignment purposes. The detectors are also equipped with a second set of fiducials for operator verification which are viewed through fixed optical fiducials mounted into the transfer platens. In this way, the operator is required to validate the relative alignment and orientation of the detector pairs and the jigs.

Mechanical assembly steps A detailed step by step description is to be found in a separate report[11-91]. A brief overview is produced here with reference to Figure 11-105.Each of the two vacuum chucks mounted on the two rotate stages (R1 and R2) are equipped with short (<300 μm) dowel pins to provide an approximate initial position for the silicon wafers which minimises the time required to locate a specific fiducial. The detectors are placed track side up on these vacuum chucks. All of the detectors are processed with sets of alignment fiducials arranged such that they are asymmetric. Detector 1 is aligned with respect to fiducials fitted into the bear-



Details of Fiducials for Automatic Alignment

Figure 11-104 Fiducial pattern on silicon wafers.

ings in the wall and detector 2 is then aligned to detector 1. These two items are then transferred to TP1. Each of the platens is equipped with further fiducials to allow additional checking of correct placement. This process is then repeated for the second set of detectors. TP1and TP2 are identical platens.

The baseboard, which is complete with its pyrolytic graphite inserts, has adhesive applied to both surfaces, and is located into transfer platen 3 by means of its precision holes. A sandwich consisting of TP1, TP2 and TP3 is constructed and is stored horizontally to allow the adhesive to cure. When this has taken place the assembly of three platens is separated, leaving the module consisting of the 4 detectors and the baseboard mounted in TP3. A complete, tested hybrid is then mounted into a support frame and adhesive is applied. This entire assembly is then mounted into TP3 and left to cure. This is repeated for the second hybrid. The completed module is removed from TP3 and fitted into its bonding/storage frame. At this point the remaining bonding and hybrid interconnect are completed. The time taken for this process is estimated to allow for production rates of at least two modules per day, at a site working a single 8 hour shift. This is well within the requirements of the total SCT construction timescale.

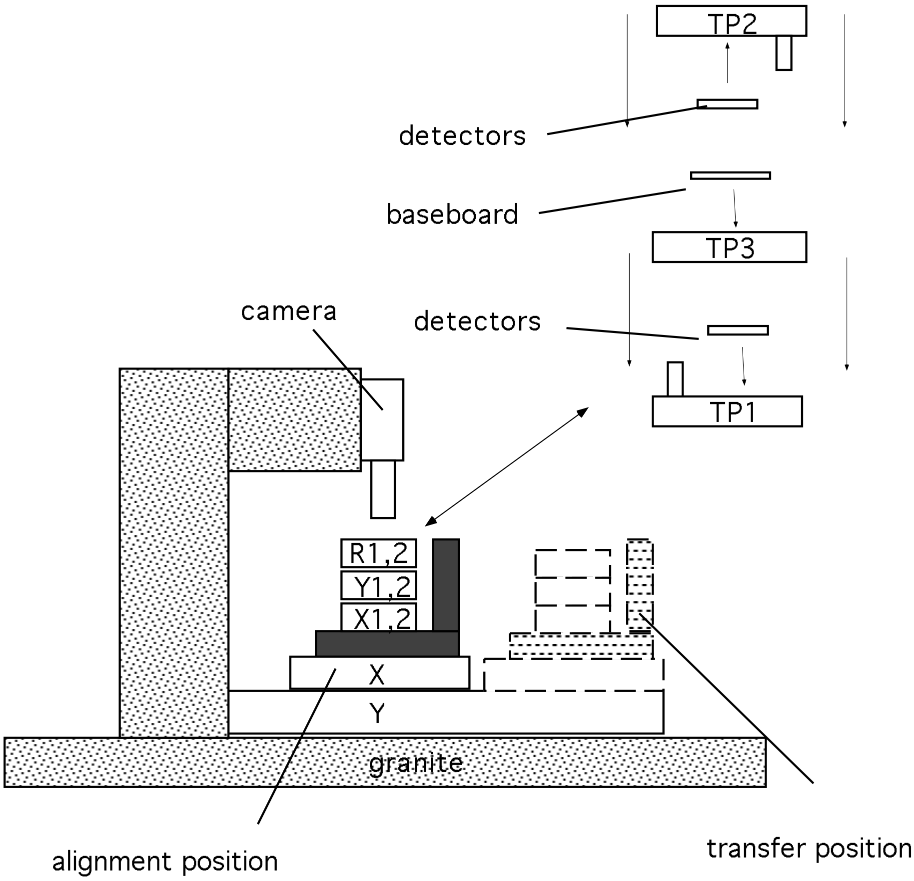


Figure 11-105 Module mechanical assembly system showing fixture definitions.

Mechanical assembly control system A more detailed description of the operation of the software may be found in reference [11-92]. The overall reference is provided by the fixed camera position. The module components are positioned with respect to pins that locate through the baseboard reference bushes. The pattern recognition system allows the centre of a circle to be accurately measured. It is assumed that both the stages and the plate with the alignment/transfer pillars have already been adjusted such that they are orthogonal to the camera axes.

The theoretical position of all the fiducials on the various plates and pillars are known. The initial positioning of the detectors on the alignment chucks is mechanically controlled to about 50 - 60 μm by positioning the cut edges of the detectors against dowel pins.

Sequence The vacuum chucks are moved to a position to allow loading of detectors. The stages will travel towards the operator until the camera optics have been cleared. The pair of detectors are then placed on their respective vacuum chucks. The vacuum is applied and the stages moved to a position under camera to find the two reference fiducials [11-91, 11-92]. It must be impossible for the operator to progress pass this point until both the detectors are held under adequate vacuum. At this stage, the computer system will require human validation of the measured pressures before the alignment process can continue. The orientation of the detectors is also checked at this stage. The detectors are placed in a position under the camera and adjacent to the position of known detector fiducials. Digitised images of the background are then recorded. Since the colour of each detector may be different, it is necessary to obtain a background reading for each of the detector fiducial areas. Since the positions of the fiducials are known it follows that the position of the background areas can be defined, and hence the motion required to reach these positions must also be known. The first detector is rotated so that its fiducials are correctly aligned to the reference frame. The fiducial positions are determined after subtraction of the background levels previously recorded. A more complete definition of the image manipulations is given below. This is repeated for the second detector. If in either of these two operations, a maximum time or a maximum number of iterations was exceeded it would be flagged as an error and the operator would be given a list of options (for example, to use an alternative set of fiducials because one of the chosen sets was damaged or missing). The first detector is moved to the correct position, with respect to the alignment fiducials. The second detector is aligned to the first. A check is made that both are still correctly aligned with respect to the reference positions Ref. 1, Ref. 2. Finally, the two chucks are moved, by the large X and Y stages to a position to allow the pick-up of the detectors onto a transfer platen.

Image manipulation description

1. Record a background image.
2. Record a fiducial image.
3. Convert both to monochrome.
4. Subtract the background from the fiducial image.
5. Apply a defined threshold and convert to 1- bit binary representation.
6. Fit bounding boxes with defined dimensions to any objects of suitable size.
7. Starting with any of the bounding boxes, find the centre of each.
8. Beginning with any bounding box centre search for two others which satisfy the criteria of correct distance and relationship.

Having found three, find the mid-point of the hypotenuse. This is the centre of the fiducial pattern.

11.10.3.6 Module electrical assembly

Following the mechanical assembly and curing of glues, a set of electrical connections are required on the module. The first are the high density wirebonds from the fan-ins to the detectors and from crystal to crystal. There are a total of 3072 of these bonds per module. This step will occur on a dedicated automatic wirebonder at each construction site. With 80 µm pitch there will be no problem bonding under fully automatic control. Particular care is, however, required to bond from the step down between fan-ins and detectors, which is just under 1 mm. Bonding will be done at room temperature using 25 µm thick aluminium wire. It is estimated that two complete modules can be bonded and inspected in one 8 hour shift. The bonding process will be able to keep up with the module mechanical construction. Many sites have access to or experience with the Kulicke and Soffa model 1470/8 bonding machines. It is likely that the majority of sites will use these units in production.

Following the wirebonding, a set of individual connections have to be made to properly supply bias and return current from the detectors. In the case of bias, an electrical connection will be made with a radiation qualified conducting epoxy for a conducting tab which is laminated inside the module sandwich to an appropriate pad on the hybrid. The ground return is wirebonded from the bias ring on the track side of the detector to a trace on the fan-in and then into the pre-amplifier ground contact.

11.10.3.7 Module test

Following the electrical assembly, all modules will undergo a set of inspections and tests to verify that they function and meet the SCT construction specifications.

A series of electrical tests will be applied to each module to check its performance and assembly yield.

1. The first electrical test will be to measure the bulk leakage current versus bias voltage. This global test is sensitive to gross problems with detector function. The measured leakage immediately after assembly also provides a reference level for each module.
2. Modules will be read out using the DAQ system and charge will be injected into each channel and binary threshold will be scanned. This is the basic test sequence which provides a measurement of noise, threshold, and gain for each channel. Nearly everything interesting about individual channels can be determined by this set of measurements. The noise per channel determines whether wirebonds are broken or missing since the strip capacitance is a significant and easily measured effect. Hot or dead channels can also be located by the noise value. In some cases, neighbouring channels may be shorted together due to bonding problems or bridging on the fan-in or on the silicon. In this case a characteristic distortion of the threshold curves on adjacent channels will be observed. In response, some bridges can be opened with a micro-probe and manipulator. The estimate for these electrical tests is 4 hours/per module.
3. Using a beta source such as ^{90}Sr or ^{106}Ru a scan of module response to ionizing radiation can be made. This is an alternate method of determining the state of each channel. It is more direct than the noise measurement but also requires additional time and overhead. By source scanning at multiple locations along the strips the alignment of the two sides of the module can be checked independent of the optical inspection system. This measurement is illustrated in Figure 11-106. About 4 hours is estimated for these source scans. An LED may also be used to scan module response. This however will not provide an alignment check as well.

All electrical measurements will be recorded in the module assembly database to be used as a future reference.

Mechanical survey This will consist of an optical inspection under a measuring microscope. It will utilize the same optics and readout as the assembly system. In addition, the module will be inspected for visual defects or damage which may have occurred in assembly or handling.

Thermal cycling While not precisely specified at present, modules will be subjected to thermal cycling over the expected range for ATLAS.

Rework Modules which exhibit electrical problems may be candidates for some limited rework. Again the potential gain has to offset the chance for reduced overall reliability. Rework will be applied in only well specified cases and documented.

Burn-in Sets of modules will be operated for the canonical 100 hours, probably at both elevated and ATLAS operating temperatures. Again, burn-in schedules will be modified based upon what is learned during the pre-production phase.

Re-test Electrical functions will be re-tested before releasing modules to the next step in the assembly sequence.

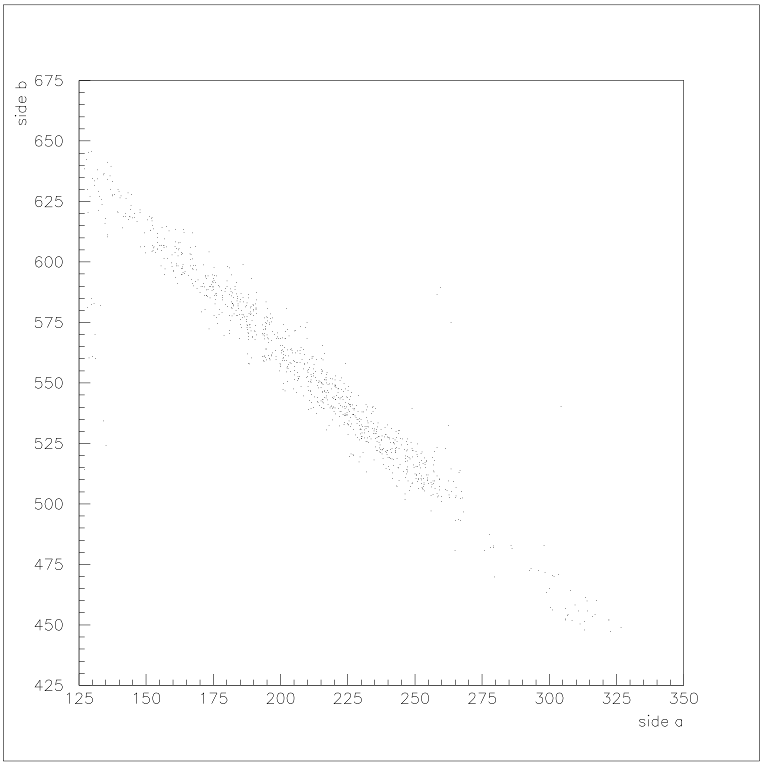


Figure 11-106 Source alignment check.

11.10.4 References

11-90 http://h2.ph.man.ac.uk/groups/atlas/SCTdatabase/Database.html

11-91 M.D. Gibson, “Proposed ATLAS Barrel Centre-tap Module Assembly Process”, Internal document, ATLAS/RAL/01/97, Jan. 1997.

11-92 M.D. Gibson, “Motion Description for Software Design”, Internal document ATLAS/RAL/02/97, Jan. 1997.