11.4 Readout Electronics

11.4.1 Introduction and Effect of LHC Environment and Operating Parameters

The SCT readout electronics is responsible for supplying strip hit information to the ATLAS second level trigger and the data acquisition system. No information will be supplied to the first level trigger. The nature of silicon micro-strip detectors necessitates that the front-end electronics be mounted immediately at the silicon strip electrodes to ensure the low noise operation required. The electronics, therefore, must be in the active volume of the detector. This dictates that front-end electronics must be of low mass. Since heat removal requires material, low power consumption is required. The electronics must also control the operation of the SCT, provide the necessary power for the electronics and detector bias, provide means for calibration and provide monitors of all aspects of the SCT operation.

The LHC operating conditions also present several challenges to the electronics for the SCT. The most obvious is the radiation environment. The expected radiation fluences are as for the silicon detectors and have been discussed in Section 11.2.3. The beam bunch crossing rate of 40 MHz and the high luminosity result in expected occupancies in the SCT up to 0.6% every 25 ns caused by real tracks. In order to simplify track reconstruction, it is important to associate each hit to a specific beam crossing. The limit on noise hits has been set so as make them a negligible addition to the expected occupancy.

The combination of occupancy and crossing frequency also dictate the bandwidth needed to transmit the data off the detector. In order minimise material and cost, data compression is required on the detector and the readout architecture is event driven. That is, data is only transmitted off detector in response to a Level 1 Accept signal for a specific beam crossing. Data is held in on-detector buffers for the duration of the Level 1 latency (<2.5 μs) waiting for the decision to transmit the data or discard it.

Another aspect of the SCT which greatly affects the electronics design is its inaccessibility. To minimise the need for repair access, the system is designed to be highly reliable, with redundancy where possible and a small loss of data from any single failure where it is not. The electronics are also designed to provide sufficient monitors and modularity of controls so that problems can be detected and corrective action taken before extensive damage is done to the SCT.

The design of all components of the SCT readout electronics from the ICs to the cables, transmission links and off-detector electronics is a delicate balance between optimising performance parameters such as noise, detection efficiency, bandwidth and reliability while minimising power consumption, material and cost.

11.4.2 Specification

The specification for the key parameters of the SCT readout electronics are listed in Table 11-12 and discussed briefly below. The parameters discussed here apply mostly to the readout electronics as a system and have obvious implications for detailed specifications of all components. The detailed specifications for particular components will be discussed in appropriate sections and found in the references.

Table 11-12 Specifications for the SCT readout electronics.

Parameter	Specification
Noise	< 1500 e^-
Efficiency	99%
Occupancy due to noise	5×10^{-4}
Bunch crossing tag resolution	1 bunch crossing
Occupancy due to real hits captured in extra bunch crossing slots	1% of real hit occupancy
Double pulse resolution	50 ns for 3.5 fC signal following 3.5 fC signal
Large charge recovery time	1 µs for 3.5 fC signal following 80 fC signal
Maximum average L1 trigger rate	100 kHz
Minimum L1 trigger spacing	2 bunch crossings
Pipeline length	128 locations
Depth of de-randomising buffer	8 locations
Voltage compliance	± 5% of nominal
Operating temperature	± 2.5 ˚C of nominal
Functionality temperature range	-15 ˚C to 30 ˚C
Power dissipation	< 3.8 mW/channel
Radiation total dose	2×10^{14} n/cm^2 10 Mrad

Noise
The front end system must provide a sufficient signal-to-noise ratio to ensure a good efficiency and low noise occupancy. The equivalent noise charge (ENC) for the front-end system is defined including the silicon strip detector parameters. The ENC defined this way is substantially larger than the pure electronic requirement on a single front end channel.

Occupancy due to noise
The noise occupancy is required to be significantly less than the real hit occupancy to ensure that the noise hit rate does not affect the data transmission rate or track reconstruction. A noise occupancy of 5×10^{-4} requires that the discrimination level in the front end electronics is set to 3.3 times the rms noise.

Timing resolution
To minimise the data to be read out and to simplify tracking, unique crossing identification is required. The silicon charge collection time of 10 ns then mandates edge-sensing discriminators, with a maximum time walk of 16 ns for the nominal threshold setting and full range of input signals. The fraction of outputs shifted to the wrong beam crossing is required to be less than 1%.

Double pulse resolution
In an edge sensing system, double pulse resolution affects efficiency. It is required to be 50 ns to ensure <1% data loss at the highest design occupancies.

Large charge recovery time

A low rate of events resulting in large charge deposition due to slow particles is expected. Therefore, although not very critical, it is desirable that the recovery time after large overloads is limited.

Trigger

The front end electronics operates at an average trigger rate of 100 kHz. The ATLAS requirement is for a 75 kHz trigger rate upgraded to 100 kHz, but because of its highly integrated nature, the full SCT electronics chain is designed for 100 kHz. The minimum spacing between consecutive triggers is 2 bunch crossings; statistical variations in trigger arrival beyond this must introduce <1% data losses for 1% occupancy. This drives the specification for the bandwidth of data links and the depth of the derandomising buffer.

Pipeline length

The pipeline length must correspond to the maximum trigger latency specified by the trigger system. With contingency, this is 3.2 μs which corresponds to 128 locations of the pipeline.

Voltage compliance

Significant voltage drops along the power distribution cables are incurred to reduce the amount of material in the sensitive area of the tracker. This requires the front end electronics to be insensitive to a bias voltage variation of ± 5% of the nominal values.

Temperature

The electronics must operate without recalibration within ± 2.5 ˚C of its nominal value. In order to allow testing at room temperature it is required that overall readout system has full functionality in the temperature range between -15 ˚C and 30 ˚C.

Power consumption

The power consumption given in Table 11-12 is the maximum permissible for the on-detector electronics. This is the number used in the design of the cooling system. The actual power consumption is estimated to be between 3.0 mW and 3.2 mW per channel, including the optical interface (Section 11.4.6).

Radiation

The total radiation levels are specified separately for the displacement damage as a fluence of 1 MeV equivalent neutrons and for ionising radiation as a dose absorbed in $Si0_2$.

11.4.3 System Design

The SCT readout electronics can be sub-divided into the following component systems:

Front-end Electronics, Links, Cables, Power Supplies, Detector Control System (DCS) and Monitoring. These are described briefly here and in detail in the following sections. The Off detector Readout and Control is described in detail in Chapter 13.

Figure 11-33 shows a schematic of the various electronic subsystems making up the SCT.

The front-end electronics include all the integrated circuits and other components that are mounted onto hybrid assemblies which become part of each detector module. These ICs perform the initial amplification of signals, discrimination, pipeline buffering, data compression and formatting the data for transmission. Diagnostic and test capability is provided in the front-end ICs (such as variable charge injection into the front-end pre-amps) but these are kept to a minimum to keep chip size and power to a minimum.

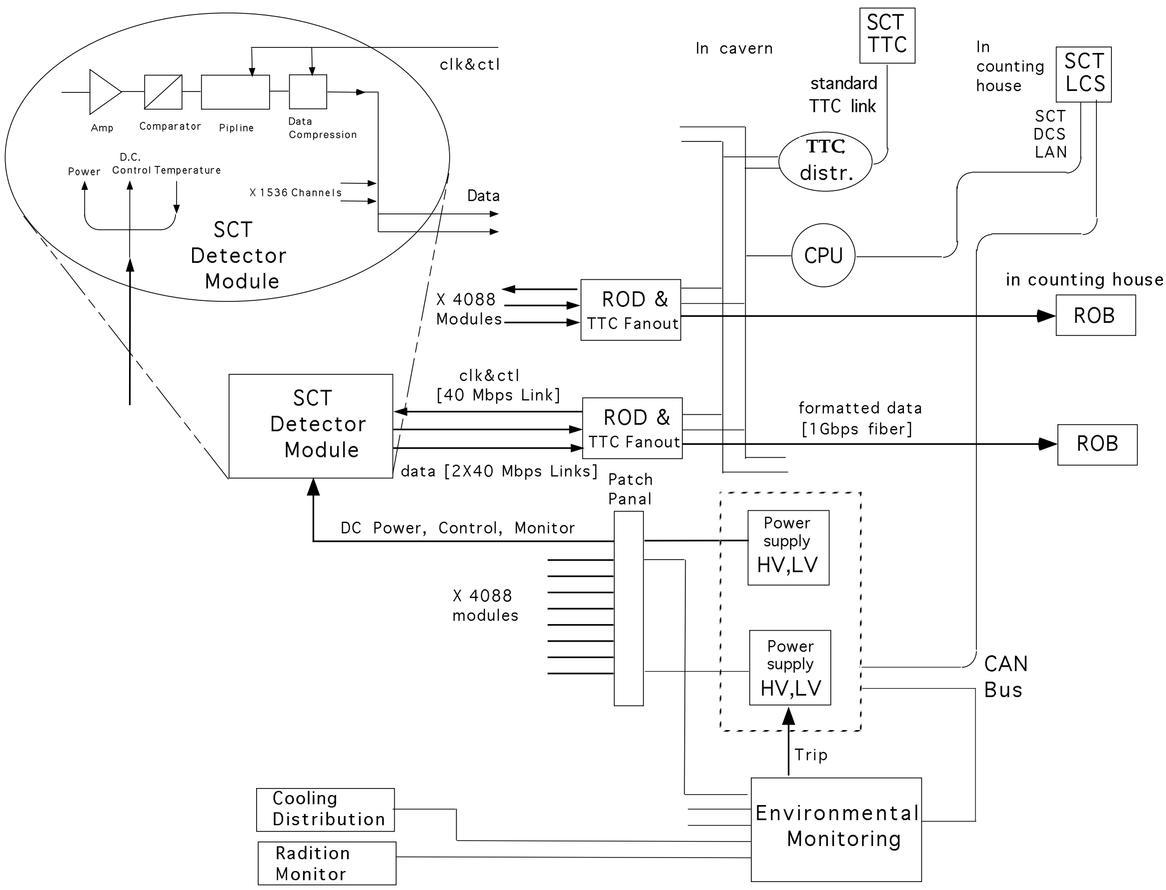

Figure 11-33 Schematic of SCT Electronics sub-systems.

Data links transmit the data off detector. Other links transmit clock and control signals to the detector. The system is highly distributed with individual links going to each module. This multiplicity matches the necessary band-width with a highly parallel architecture to enhance the reliability of the SCT. Standard commercial links are not practical for this application, therefore the design employs 40 MHz links developed specifically for this application.

The cable system provides all power and DC control signals to (and from) the detector modules from power supplies located off the detector. Individual cable paths are provided for each detector module. Segmenting the power distribution to each module offers a more robust system in that any single failure will disable only a small fraction of the SCT. It allows silicon bias to be adjusted for variations in radiation dose and monitoring of currents and control of voltages to each module. Inside the detector volume, the cables are made of low mass aluminium on Kapton. Outside the detector they are of conventional twisted pair construction.

The off detector readout and control system is the interface between the SCT detector modules and the ATLAS Data Acquisition (DAQ) System and the ATLAS Trigger, Timing and Control (TTC) System. There are two main functional blocks; the Readout Driver (ROD) and the SCT-TTC distribution. The RODs receive data from the detector modules, interpret the SCT protocol, monitor for errors, reformat, buffer the data and feed it to the ATLAS standard Readout Buffers (ROB). The SCT-TTC interfaces to the ATLAS standard TTC. It receives clock and control information from the TTC, decodes the subset required, reformats and distributes it to the SCT-TTC links using the SCT protocol.

The power supplies provide all necessary power to the front-end, on-detector electronics and to bias the silicon detectors. This subsystem also includes a few necessary DC control signals required by the on-detector electronics. Each module has separate individual supply channels and current monitoring. This ensures a robust system and allows control of grounding.

The SCT-DCS is the interface between the SCT and the ATLAS general DCS. It interfaces the power supplies, the off detector readout and control system, the various monitoring systems, and the alignment and cooling systems to the centralized ATLAS control system. It also provides a means for locally controlling the SCT independent of the ATLAS DCS and will allow stand alone running of the SCT before integration into the complete ATLAS detector.

Monitoring functions in the SCT are widely dispersed, both in the physical distribution of the sensors and in the distribution of the initial destination of the information. Electrical performance of the detector modules is monitored via the power supplies measuring currents and voltages. The leakage current of each detector is also a good measure of temperature once it has been calibrated, but there is also one temperature probe (RTD) on each detector module. Additional temperature monitors accompany the cooling system inside and outside the detector volume. There are further temperature, humidity and pressure sensors associated with the alignment system. Separate radiation monitors monitor beam focusing problems. All of the monitoring systems feed data into the SCT-DCS.

Those monitors which track characteristics that may have an impact on the safety of the detector have separate hardware connections to trips which will protect against damage to the SCT.

11.4.4 Front-end Integrated Circuits

The basic front-end architecture is shown in Figure 11-34. The chosen architecture is 'binary', in which the signal from the silicon strip is amplified, shaped and discriminated yielding only hit/no-hit information for each bunch crossing. The following functions are provided by the front end electronics:

- detection of hits above the noise level for a given beam crossing,
- readout of three bunch crossings, centred on the L1 trigger,
- switchable discrimination, between level and edge sensitive,
- storage of hit patterns for L1 trigger latency,
- de-randomising buffers,
- sparse, data-driven, readout of data upon receipt of L1 trigger signal,
- calibration pulse injection,
- redundant data readout paths,
- set-up and reset modes for normal data taking,
- set-up modes of operation for DAT system and clock synchronisation,
- x-ray mode of operation for use with x-ray survey beams,
- masking of bad strips.

Hits above threshold recorded by the discriminator are stored as single bits in the binary pipeline for the L1 trigger latency. Upon receipt of a L1 trigger signal, the sparse readout of hit pat-

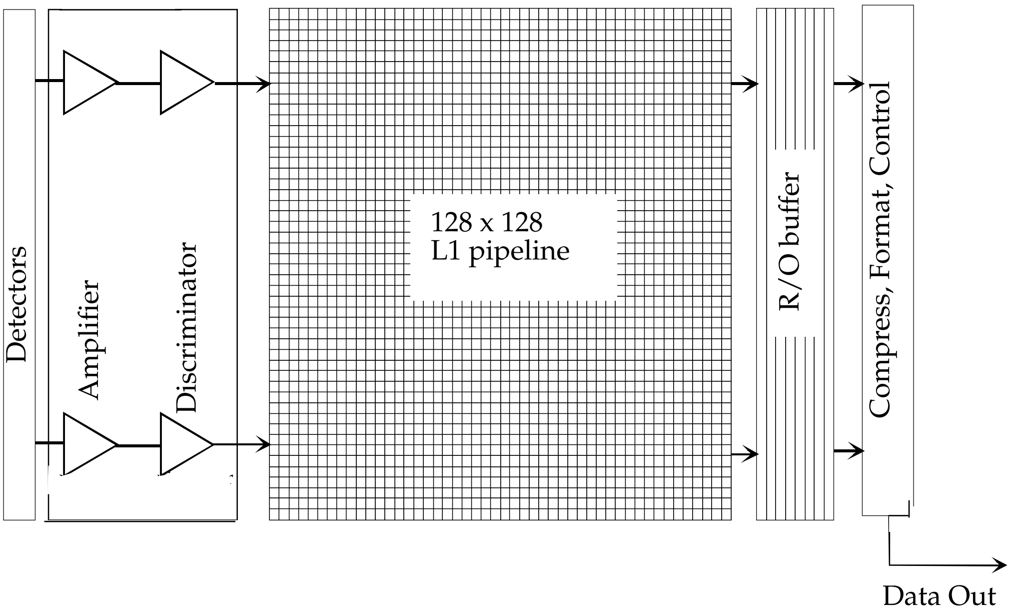

Figure 11-34 On-detector Front-end architecture.

terns from pipeline cells corresponding to a given bunch crossing is performed. In one mode of operation the discriminator edge-senses, recording one hit per bunch crossing. In this mode, dead time associated with the analogue chain results in the detector being insensitive to the subsequent bunch crossing after a hit. There is an alternative mode of operation in which the discriminator is level sensing. Three bunch crossings are readout around each hit, which results in the efficiency being slightly better but the noise occupancy correspondingly worse.

Efficiency and noise occupancy in this system rely strongly on the signal-to-noise ratio provided by the front end circuit and on the matching of amplifier gains and discriminator thresholds. Given the requirements concerning the noise and speed performance, power consumption, matching of gain and discriminator offset and radiation hardness, a bipolar technology is preferable for this part of the front end electronics. The pipeline and the sparse readout circuitry are realised in a rad-hard CMOS technology. A modularity of 128 channels per chip is chosen. In order to minimise interference from data readout activity, communication between chips uses standard Low Voltage Differential Signals (LVDS). DC control lines are not constrained to this protocol.

The number of suitable technologies which satisfy the requirements, particularly those concerning radiation hardness, is very limited. Based on the extensive development program two technological options have been identified. In the first, the functions of the front end electronics are split into two chips: an analogue chip (CAFE-M) containing the preamplifier, the shaper and the discriminator realised in a bipolar technology (CB2 process by MAXIM), and the ABC pipeline chip [11-35] realised in a CMOS technology (RICMOS-IV process by Honeywell). The second option is based on the DMILL BiCMOS technology, which offers the unique feature of combining high performance radiation hardened bipolar devices with radiation hardened CMOS devices. The DMILL process allows all functions of front end electronics to be fabricated in a single chip (ABCD). These two technological options are considered at the present stage as two vendor options for the final readout electronics for the SCT. With respect to the electrical parameters and logical functionality the designs implemented in both options are fully compatible.

The two technology options are, however, substantially different and therefore detailed implementations of some blocks are different for each option. They use the same power distribution system, data transmission and off detector electronics. Since one option results in having the front end functions split into two chips and the other includes all functions in a single chip some geometrical differences in the hybrid designs for these two options are unavoidable.

11.4.4.1 Analogue front end

The block diagram of the analogue signal processing chain is shown in Figure 11-35. The preamplifier circuit is based on a transimpedance amplifier configuration with a bipolar input transistor since for large detector capacitances and short shaping times bipolar devices offer a superior noise versus power figure of merit. The input stage is followed by a single gain stage and an integrator providing the proper peaking time. A key issue for the binary architecture is the channel-to-channel matching of gain, noise, DC level at the shaper output and the discriminator offset since a common discrimination threshold is applied to all 128 channels in a single chip. The required uniformity is obtained by:

- an ac coupling between the amplifier and the discriminator so that the DC offsets originated in the front end circuit, which is a single ended structure due to noise requirements, are cut off,
- high enough gain in the preamplifier-shaper circuit, of 100 mV/fC, so that the input offsets in the discriminator are negligible compared to the signal amplitude, and
- applying a differential scheme for setting the discriminator threshold so that common mode effects are suppressed.

Calibration of the front end electronics can be performed using the calibration scheme implemented in the front end chip. A calibration capacitor of 100 fF is placed at the input of each channel. Each calibration input is connected to one of four calibration buses with every fourth channel connected to the same bus. This allows calibration pulses to be injected either by applying voltage steps directly to external pads or by using the internal calibration circuit which generates calibration pulses in response to a programming command.

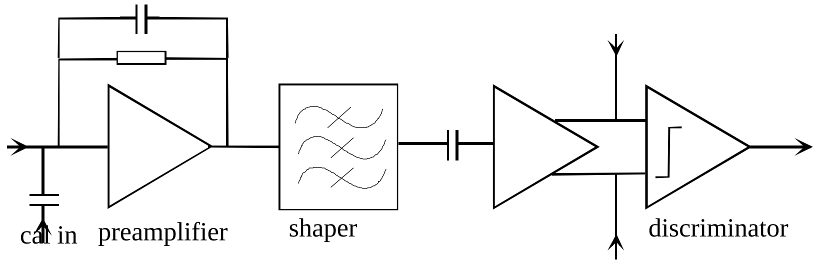

Figure 11-35 Block diagram of the analogue front end circuit.

A number of prototype designs following the architecture shown in Figure 11-35 and with parameters close to those required for the SCT readout have been developed, in particular the FABRIC chip [11-36] used in NA50 experiment at CERN, the LBIC [11-37] and the CAFE [11-38] prototypes and the SCT128B chip [11-39] developed in the DMILL technology. Based upon previous work the final designs for both technological options have been completed. In the case of using the MAXIM bipolar process this is the CAFE-M and in the case of using the DMILL process this is the front end part of the ABCD chip. The detailed specification for the CAFE-M chip is described in [11-40]. The front end part of the ABCD design follows the same specification except those which concern specific functions of CAFE-M related to the two-chip system and which are not required for the ABCD chip.

11.4.4.2 Noise performance

A target value for the SCT readout system is a signal-to-noise ratio of 12 at the end of the detector lifetime. In order to evaluate properly the noise performance of front end electronics one has to take into account several effects:

- electrical parameters (capacitances and strip resistance) of silicon strip detectors,
- ballistic deficit due to charge collection time,
- noise injection from neighbouring channels,
- radiation damage to detectors and to electronics.

The electrical parameters of silicon strip detectors assumed for the front end design are listed in Table 11-13. Strips of 12.8 cm length with front end electronics connected in the center, as for the centre type module, are considered as a basic electrical unit. The detector design using the n-side strips results in a relatively large detector capacitance of 1.5 pF/cm and total of 19.2 pF for unirradiated detectors. For irradiated detectors when they pass the type inversion point the ohmic side becomes the junction side and the interstrip capacitance is lower (see Table 11-13), resulting in a total input load capacitance of 15.4 pF.

Table 11-13 Electrical parameters of detectors assumed for the front end design.

	Unirradiated	**Irradiated**
Coupling to amplifier	AC	AC
Coupling capacitance	20 pF/cm	20 pF/cm
Capacitance of strip to all neighbours	1.22 pF/cm	0.92 pF/cm
Capacitance of strip to backplane	0.28 pF/cm	0.28 pF/cm
Metal strip resistance	15 Ω/cm	15 Ω/cm
Bias resistor	750 kΩ	750 kΩ
Maximum leakage current per strip	2.0 nA	2.0 μA

The signal-to-noise ratio or the ENC for used here is for the full equivalent model of a reference silicon strip detector and several channels of electronics connected to it [11-41]. The diagram illustrating how various effects contribute to the final signal-to-noise ratio is shown in Figure 11-36.

For a given detector capacitance and a given shaping time in the case of front end electronics using a bipolar transistor as an input device, there is an optimum collector current resulting in minimal noise. This is a matter of a proper balance between the voltage noise contribution which is inversely proportional to the collector current and the parallel noise contribution which is proportional to the collector current. The optimum value of collector current depends on the current gain factor β of the input transistor. Since β will be degraded by radiation dam-

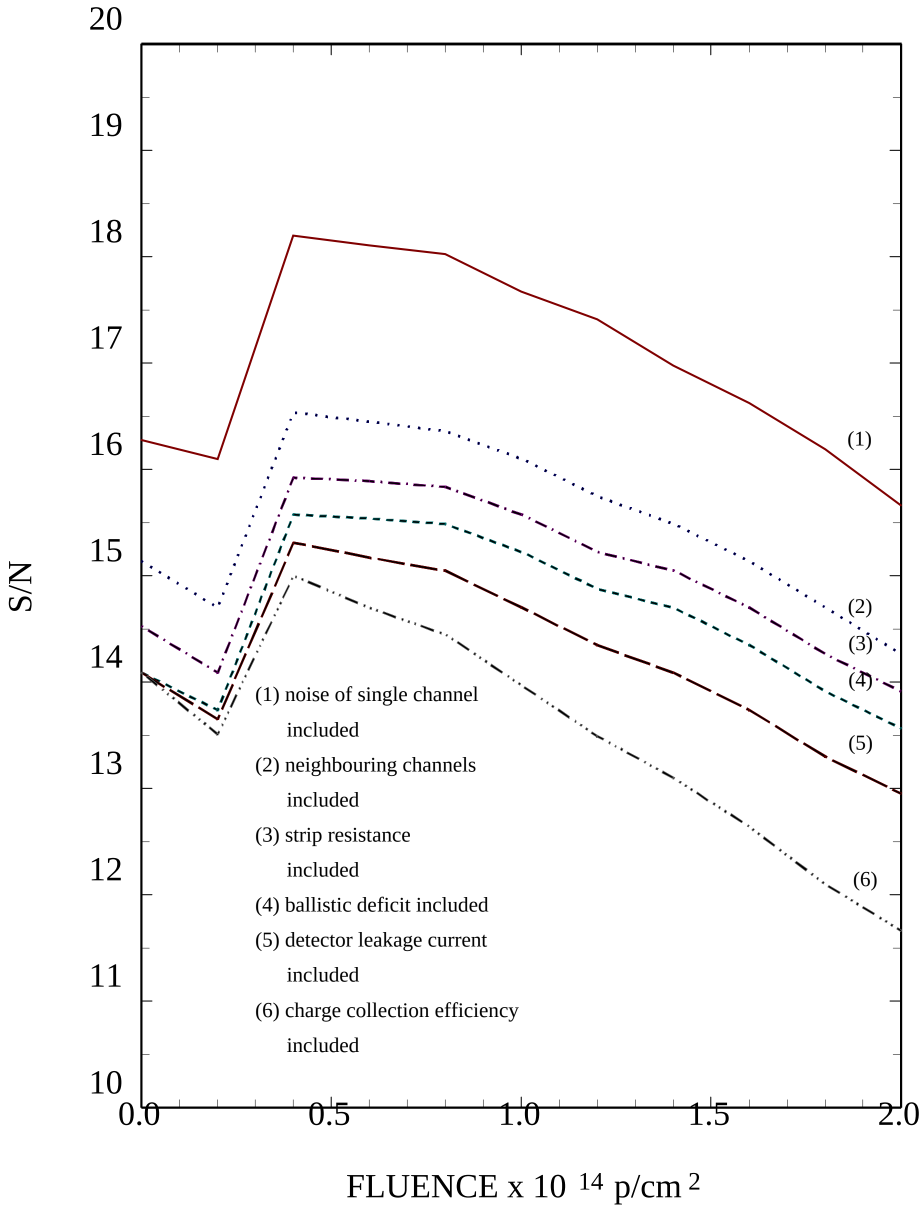

Figure 11-36 Composition of equivalent noise charge for silicon strip detector readout.

age it is foreseen that the collector current in the input stage will be changed during the experiment lifetime. The detailed discussion of front end optimisation is presented in [11-42]. The radiation effects will be discussed in Section 11.4.6.3.

11.4.4.3 Timing performance

Three critical timing parameters are determined by the performance of front end electronics:

- timewalk of the discriminator,
- double pulse resolution,
- recovery time for overloading pulses.

For the implemented discriminator, the time walk depends in a straightforward way on the peaking time of the shaper preceding the discriminator. For the ideal case, the peaking time of 25 ns selected is sufficient to meet the requirement for a timewalk of 16 ns. A critical parameter, however, is the minimum overdrive which still provides an in-time response. In order to meet the requirements, this is specified as 0.25 fC which means that signals with amplitudes between 0 and 0.25 fC above the threshold are allowed to produce responses captured in the following beam crossing slot. These are mostly pulses associated with hits giving good signals with the correct timing on one strip and very small signals on the neighbouring strips.

The simulation results illustrating the timing performance of the front end electronics are shown in Figure 11-37. Plot (a) shows the delays of the discriminator response for input signals of 1.25 fC, 2 fC, 4 fC and 10 fC while the discriminator threshold is set at the nominal level of 1 fC. Plot (b) shows the double pulse resolution for two signals of 3.5 fC each spaced by 50 ns. Plot (c) illustrates the large signal recovery time. A nominal signal of 3.5 fC comes 1 μs after a large signal of which leads to saturation of most of front end circuits.

11.4.4.4 Input register and pipeline

The input register provides two functions: edge sensing or level sensing of signals delivered from the discriminators, and the masking of channels. The data from the discriminator outputs is sent to a edge sensing circuit which generates only a single "1" for every hit detected by the discriminator irrespective of the pulse duration at the discriminator output. This function can be disabled by a programming command and then the data will be written into the input register in the level sensing mode. The mask register is used for disabling any bad or noisy channels. In a test mode the register can be used to apply test patterns to the pipeline.

The mask register outputs are sampled at each bunch crossing and stored in the pipeline. The implementation of the pipeline in the ABC chip and in the ABCD chip is different. The design most suited to the technology is used in each case. In both cases the pipeline provides the same function.

In the ABC chip [11-35] the pipeline consists of 128 locations of dual ported RAM. This block of RAM is addressed by 2 circular pointers, one read and one write. The write pointer is used to address the next location in the RAM in which data will be stored. The read pointer follows the write pointer by 128 locations. When a L1 trigger is received the sample being addressed by the read pointer together with the next 2 samples are copied into the readout buffer. The pipeline structure as implemented in the ABC chip has been employed successfully in the prototype designs of CDP-64 and CDP-128 chips [11-43], both following a principle of the clock driven pipeline. The CDP-64 chip has been used successfully together with the FABRIC front end chip for the binary readout of silicon strip detectors in the NA50 experiment at CERN. The CDP-128 chip has been used extensively in conjunction with the LBIC front end chip and the CAFE front end chip in the SCT beam test program.

In the ABCD chip the binary pipeline is realised as a multiplexed FIFO circuit. An array of 12x12 dynamic memory cells is controlled by 12 non-overlapping clock signals. In each clock cycle only 12 cells out of 12x12 are switched while the effective delay provided by such a block is equal 12x(12-1) clock cycles. The pipeline block comprises 128 channels, each 132-bit deep. The hit pattern from the input register is shifted through the pipeline during 132 clock cycles. When a L1 trigger arrives the patterns corresponding to three consecutive bunch crossings are transferred from the pipeline to the readout buffer. This binary pipeline structure has been employed successfully in the SCT32B and SCT128B chips [11-39].

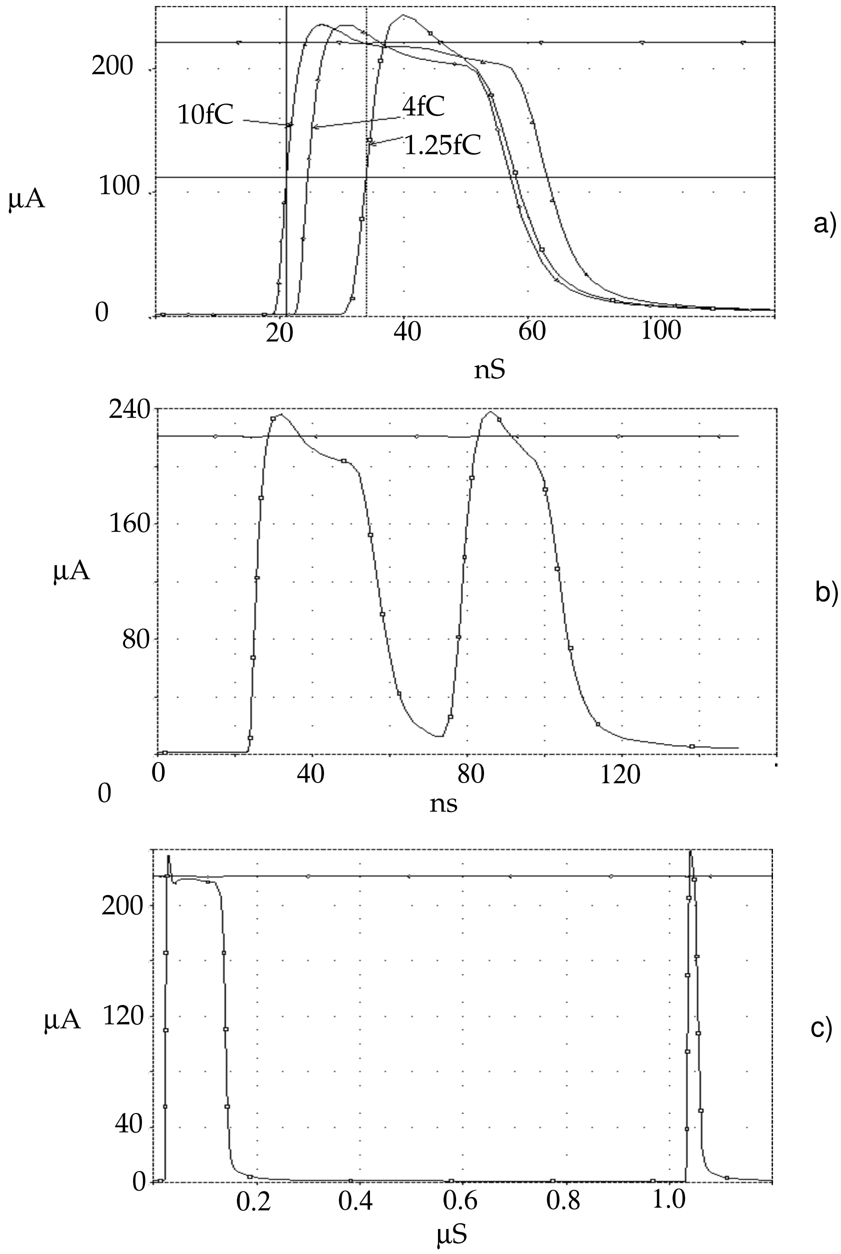

Figure 11-37 Simulated timing performance of the front end electronics: (a) timewalk, (b) double pulse resolution, (c) large signal recovery time.

11.4.4.5 Readout buffer and data compression logic

The readout buffer is a 24 location deep FIFO which serves as a derandomiser removing fluctuations from the L1 trigger time distribution. Given the 3 bunch crossing samples stored for each valid L1 trigger it has sufficient capacity to hold the data from up to 8 events without data loss. If the capacity of the readout buffer is exceeded the oldest events in the buffer are overwritten by new ones. Logic built into the readout buffer keeps track of its content and on the events which have been overwritten. The buffer is built as 128x24 RAM. The memory is addressed by two pointers, a write pointer and a read pointer, allowing for simultaneous writing and reading.

As soon as there are data in the readout buffer to be processed the 3 bunch crossing samples that constitute an event are transferred to the data compression logic. The function of the data compression logic is to find the data from channels which have been hit and only pass this data to readout logic for transmission off the chip. The data compression logic performs a sequential search, looking for channels that have the required hit pattern. A choice of 4 hit patterns are available as listed in Table 11-14. Only data that match the selected criteria are transferred to the readout logic.

Table 11-14 Data compression criteria.

Selection criteria	Hit pattern	Usage
Any hit	1XX or X1X or XX1	Detector alignment
Level sensing	X1X	Data taking in level mode
Edge sensing	01X	Data taking in edge mode
Test	XXX	Test mode

11.4.4.6 Readout and control

The task of the readout logic on the chip is to organise the readout of data from the chip itself as well as the readout of data from several chips on the module. The module is served by 12 pairs of CAFE-M and ABC chips or by 12 ABCD chips. On each side the data from 6 chips are sent to an optical fibre interface via a single connection. The data that pass the data compression criteria must be added to an address and formatted to suit the protocol used for the data transmission. The protocol adds extra bits to the data stream, which enables synchronisation. In this system one chip is connected to the data link and programmed to be a master. The remaining five chips on one side of the module are programmed to become slaves. The last chip in the readout chain is designated as the end chip. On receipt of an L1 trigger the Master chip first outputs any data it has to send over the link. When it has completed sending its data it sends a token to the slave chip on its right. On receipt of the token the slave sends its data to the master which sends this data to the link. Once the slave has finished sending its data, it passes the token on to the next slave which then starts to send its data. This process continues until the last chip in the readout chain, the end chip, has sent its data. This chip appends a unique data packet to its data stream. When the master receives this packet it interprets it as the end of data. It is then free to initiate another readout cycle. This scheme minimises the number of connections needed on the hybrid.

In order to make the front end chip practical for use in a large system and reduce the number of service connections on the hybrid some additional functions have been implemented in the chips. The discriminator threshold can be set by an internal DAC or by a differential applied to the bonding pads. The calibration signals can be provided either via 4 external pads or can be generated internally by a programming command. In the latter case the address of one of the four calibration lines, the amplitude of the calibration pulse and the phase of the calibration pulse with respect to master clock are defined by programming commands. The programming commands as well as data for the chip configuration are received and interpreted by the readout and control logic.

11.4.4.7 Redundancy

Each chip has duplicate sets of control lines and data inputs and outputs. In the case of a chip failure, software commands can instruct the chip's neighbours to route data and control around it. DC control lines from the power supplies can instruct chips which of their clock and control lines to use. In case of failure of a data link or of a master chip, the master on the opposite side of a module can be instructed to transmit the data for both sides. In this case, the maximum occupancy at 100 kHz L1 rate is 0.95% (for a 1% data loss [11-63]).

11.4.5 Hybrids

The hybrids play a role in mechanical support, cooling, and electrical readout. In this section the readout aspect is considered.

Each module includes two hybrids, serving the two sides respectively. There are six 128 channel chip sets on each hybrid. The hybrid electrical design is similar for both the chip set options. Most of the difference is geometric since the DMILL choice is physically smaller. For the sake of brevity only the two chip solution is described here.

The hybrid circuit is patterned using a commercial thick film process. The substrate is Beryllium Oxide (BeO), which has a radiation length of 144 mm. The conductors used are gold but to reduce material they are printed thin at 8 µm. The minimum trace width is 200 µm on a 400 µm pitch. The design consists of three conductor planes and two orthogonal trace layers. The first plane is a shield layer which is grounded at one point and carries no current.

Beryllium Oxide is not as common a substrate choice as Aluminium Oxide. However it has a very high thermal conductivity (250 Watts/mK versus 30 Watts/mK for Alumina) and a long radiation length. This material has already been used for hybrids on a number previous vertex detectors at LEP and at CLEO, and in prototypes for the SCT and the CDF experiment.

The hybrids used on the two sides of a module are identical. Readout is from the "top" side hybrid. The "back" side hybrid is accessed through a wrap around cable. A basic electrical schematic of the final hybrid is shown in Figure 11-38 and a mechanical layout is shown in Figure 11-39 . The circuitry on the hybrid performs the following electrical functions:

- distribution and bypass of power and ground to the front end chips,
- distribution of clock and control to the binary pipeline circuitry,
- return of data to the off module optical transmission board,
- filtering and AC current return of the detector bias line,
- support of the redundancy functions of the digital chips and the bypass lines for chip failures.

The design and layout of the hybrid is driven by the noise and signal speed specifications from the front end chips. Its design is a critical element in the performance of a module. Signal routing and filtering is critical in this mixed analog/digital application. In addition, trace capacitance is kept to < 50 pf to minimize the excess load on the ABC chip outputs. The final hybrid is the result of a substantial prototyping program.

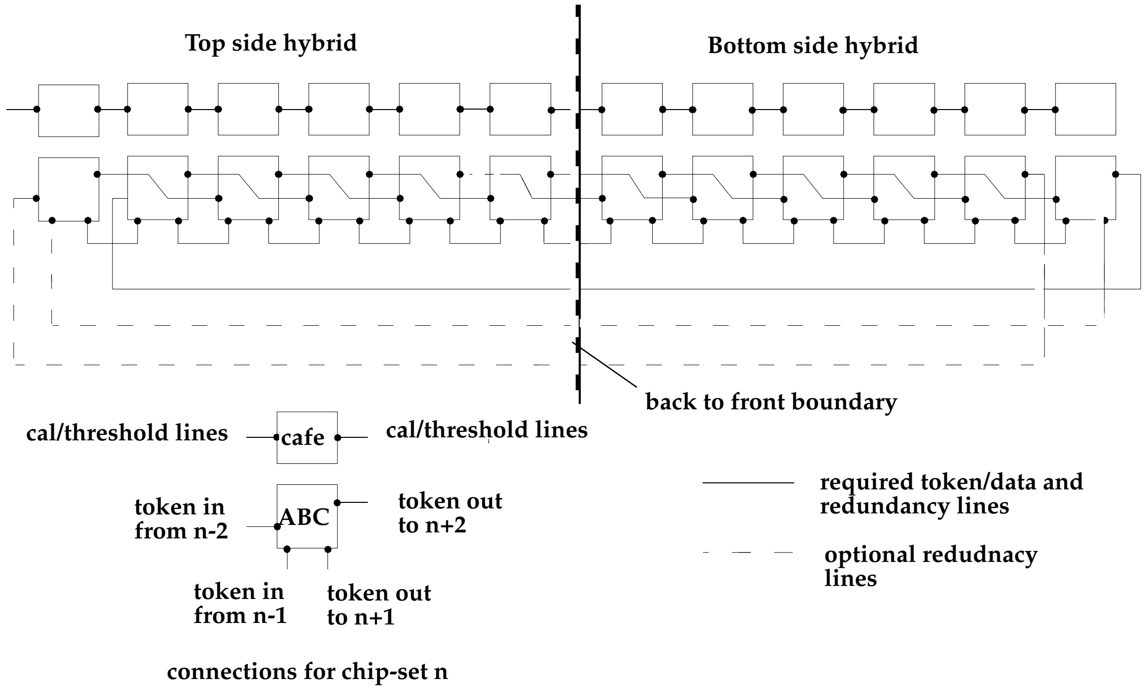

Figure 11-38 Electrical Schematic of the barrel Hybrids.

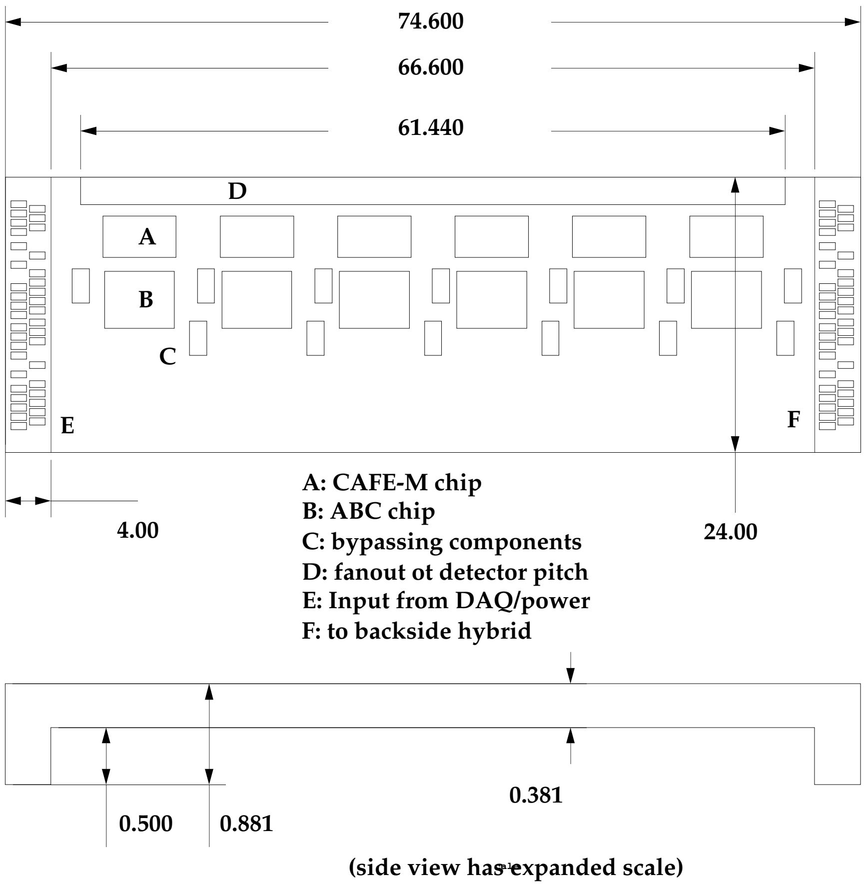

Figure 11-39 Mechanical Layout of the barrel Hybrids.

The gold conductors are a point of concern due to their short radiation length. However, the use of gold adds significantly to the reliability of the design and the assembly process. A detailed radiation length breakdown is given in Section 11.5.5.

11.4.6 Data Transmission

11.4.6.1 Requirements

The transmission of data to and from an SCT module must satisfy the following requirements:

- the transfer of a 40 MHz clock to the SCT module,
- the transfer of trigger and slow control signals to the SCT module,
- the transfer of approximately 35 Mb/s of data from the SCT module[1],
- a data loss of below 0.1%,
- operation for the full life time of ATLAS,
- a minimal material budget.

A system based on optical fibres has been designed to meet these requirements and will be described below. An alternative system based on miniature shielded twisted pair cables, as proposed for use by the TRT, is being evaluated. It has advantages in cost and radiation hardness over the optical system, but lacks the desirable possible noise immunity provided by the optical system and requires more material in the inner detector. It is being considered as an alternative, but will not be discussed further in this TDR.

11.4.6.2 System description

The design must address concerns of electronic noise, component life time, redundancy in case of component failures, fibre protection and ease of assembly. These lead to the design choices described below. The performance of a prototype link using many of the components described here will be discussed thereafter.

An overview of the system is shown in Figure 11-40. The system consists of three optical fibres per module, two for transmitting data from the module to the ROD and a third for sending multiplexed clock and command signals. Two links operating at 40Mb/s easily accommodate the data rate and provide headroom and redundancy. Light signals are generated using LEDs and received using PIN diodes. The clock and command signal is multiplexed using bi-phase mark encoding, and demultiplexed in an ASIC. The outcoming data links use an NRZ[2] encoding scheme. On the ROD end of the link a low-noise preamplifier is used to reconvert the optical signals to electrical signals, and multiplexed clock and command data are transmitted using a LED.

The fibres are terminated in a custom package containing two LEDs and one PIN diode. This package resides on a small hybrid a few cm from the SCT module, along with the drivers for the

1. The data transfer rate per module is based on assuming a maximum occupancy of 1% and a maximum L1 trigger rate of 100 kHz, leading to a nominal maximum data rate of 35.4 Mb/s.
2. Non-return to zero.

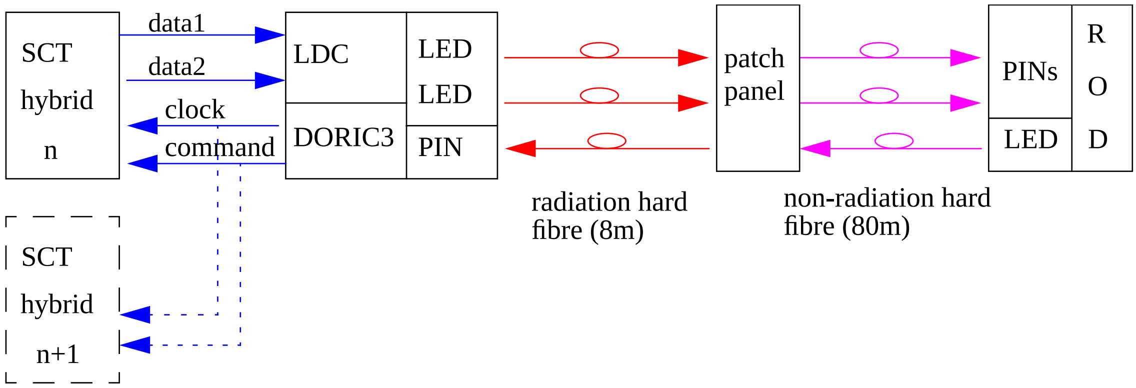

Figure 11-40 Schematic of system showing data flow and redundancy.

LEDs and the DORIC3 ASIC for demultiplexing the clock and command signals. The optical hybrid will have a short pigtailed electrical connector to the module and a fibre pigtail terminated in an MT-4 connector (described below).

Each optical hybrid receives two LVDS signals from the module and sends the clock and command as LVDS signals. The prospect of electronic noise due to pickup or ground loops between the FE chips and the optical hybrid is reduced through the use of these low amplitude differential signals. In addition attempts are made to minimize the length of the data paths between the FE and the electro-optical components.

Table 11-15 summarizes the components of the system, which are described below.

Table 11-15 Components of the data transmission system.

Component	quantity
GEC package (2 LEDs + 1 PIN diode)	4088
DORIC3 chip	4088
LDC driver chip	4088
receiver (PIN + preamp + discriminator)	8176
radiation hard fibres (approx. 8 m length)	12264
MT-12 connectors at muon crack patch panels, and at RODs	2044
12-way fibre ribbons to muon crack patch panels	1022
96-way fibre cables to ROD	128

Packaging of optoelectronics

The optoelectronics will be mounted on a small hybrid near, but separate from, the module hybrid. This optical hybrid will have a pigtail to connect to the SCT module. In addition to the data and clock and command lines, power for the optoelectronics will be derived from the module. The active component on the optical hybrid is a non-magnetic pigtailed package containing two LEDs and one PIN diode. This package, made of radiation hard materials, has been developed with GEC-Marconi (UK)[1]. The package is approximately 6mm x 10mm x 1.4mm, and in-

1. GEC 520/1/02113/000

cludes ground planes for placement of the LED driver and DORIC3 ASIC. The components of this package are described below.

LEDs

The LEDs proposed for use in the link are obtained from GEC-Marconi. They produce light at 820 nm wavelength and, at an operating current of 20mA, produce on average 17µW of optical power coupled into the pigtailed fibre. The rise and fall times are 3.5-4 ns. In addition to the 20mA drive current for transmission it is foreseen to provide currents up to 50 mA for annealing damage suffered from irradiation.

The electro-optical components must survive for several years during the construction phase of ATLAS and for 10 years during detector operation at LHC. An effort has been made to maximize LED life time by using an NRZ protocol, which minimizes the amount of time the LEDs will be run at high drive currents. The use of this protocol requires a DC-coupled system. As a further precaution the optical hybrid will have a dedicated cooling contact so the electro-optical components will operate near -10°C.

PIN diodes

The PIN diodes used for prototyping are inadequate for the final system. The response, typically 0.5 A/W at 820 nm, is adequate, but the 10%-90% rise time of 15 ns at -5 V bias is insufficient for 40Mb/s transmission. A source for epitaxial silicon PIN diodes has been found to meet the need for faster operation. The specifications are:

- a responsivity at 820 nm > 0.35 A/W,
- a 10%-90% rise and fall times at -5 V of 1 ns,
- a capacitance at -5 V < 2 pF,
- a dark current < 5 nA.

Demultiplexing chip: DORIC3

The current output signal of the PIN photodiode is DC coupled into the input stage of DORIC3, which is a low noise trans-impedance amplifier. The output of the trans-impedance amplifier is ac coupled into a differential gain stage. All of the analogue and digital circuitry following the transimpedance amplifier has been designed with low-level differential inputs and outputs to minimise feedback and make it insensitive to supply line noise and variation. A comparator produces digital outputs from the amplified signals, then a decoding circuit re-generates the clock, extracts the data and synchronises data to the clock. The bi-phase mark decoder is the biggest part of the active circuitry. Clock and data are output as LVDS compatible voltage levels. Two sets of clock and data outputs are available, the normal outputs driving the local module and reserve (or redundant) outputs driving an adjacent module, and may be switched on and off independently by means of control lines.

The DORIC3 specifications are:

- input current signals nominally 0µA and 6-12µA, of either polarity,
- supply 4 V ±200 mV, current approx 50 mA, dissipation approx 200 mW,
- control line signals 0 V ±1 V, 4 V ±1 V,
- outputs differential, low voltage swing, nominally LVDS compatible,
- operating temperature range -10 °C to 30 °C.

LED Driver Chip: LDC

The driver chip for the LEDs has two main circuit blocks, an LVDS compatible input stage and a high current output driver. Inputs will be connected to ABC outputs by plugs and sockets and wiring of indeterminate length so they must be protected against ESD. The input stage must provide adequate drive signals for the output stage. The output stage is a differential pair with a current source supplying the tail current. The tail current is adjustable from zero to 50 mA by means of an external control voltage. Five percent of the tail current is bled continuously into the LED to keep it forward biased and improve switching times. Two completely independent circuits are provided on one substrate.

The LDC specifications require:

- two independent channels,
- inputs LVDS compatible voltage levels and common mode range, each input pair internally terminated with 100 Ω, protected against ESD, compliance level to be found on test,
- output switched currents adjustable from 0 to 50 mA by control voltages,
- a control voltage range 1.6 V to 6.6 V, protected against ESD,
- supplies 4 V ±200 mV, current 2 mA to 55 mA, for each channel,
- an operating temperature range -15 °C to 30 °C.

The DORIC3 and LDC chips were designed to work with and within the size envelope defined by the space reserved for them on the GEC package. They have been submitted to a process that is not radiation-hard, but with careful design, using the most tolerant components and circuitry, the process may provide devices that are sufficiently radiation tolerant. The chips will be irradiated to determine their radiation tolerance.

Optical fibre

Radiation hard 50 μm core multimode fibre will be used between the optical hybrids and patch panels in the region between the barrel and forward cryostats, a distance of approximately 8m. From the patch panels to the electronics room, a distance of 80m, non-radiation hard fibres will be used, as these are substantially cheaper per unit length. For ease of assembly and installation the use of fibre ribbons and ribbon connectors is foreseen. The three fibres from each module will be merged into 12-way fibre ribbons. Connectors are foreseen at the outer radius of the inner detector. The MT-12 connector supplied by Europtics Ltd. would be suitable. Ribbons of radiation hard fibre will go from there to patch panels in the gap region between the barrel and end-cap cryostats (for barrel SCT modules) or at the outer ends of the forward TRT (for forward SCT modules). At this point the transition to non-radiation hard fibres will be made. These non-radiation hard fibres running to the control room could be grouped into 96-way fibre cables in protective sheaths. A final set of MT connectors will be used at the ROD.

Within the SCT itself, each row of the barrel is currently envisaged to have twelve SCT modules and twelve optical readout boards along z, with six modules read out at each end of the barrel. This is imperfectly matched to the use of 12-way connectors and ribbons, but could be accommodated by either reading out different numbers (8 and 4) of modules at each end of the barrel, alternating long and short rows, or by merging fibres from adjacent rows into the same connector. The modules will be pre-cabled with a set of fibres of appropriate length to be regrouped onto MT-12 connectors at the barrel patch panel. The forward SCT modules can also be conveniently grouped in fours onto MT-12 connectors at the forward patch panel. 12-way ribbons can be used to reach the outside of the detector. From there matrix assemblies of 12-way connectors will allow regrouping into 96-way non-radiation hard fibre cables.

Off-detector receiver

The data signals will be received by a high response silicon PIN diode followed by a low noise trans-impedance amplifier designed for opto-electronic receivers [11-44]. A discriminator will need to be added to this preamplifier.

11.4.6.3 Radiation hardness

It is clear that LED+PIN optical links operating at 40Mb/s exist in low-radiation environments. The testing of these links after irradiation, however, is crucial. Significant effort has gone into irradiation studies of LEDs. The properties of optical fibres and PIN diodes after irradiation have also been studied. Only those aspects directly relevant to the proposed SCT data transmission system will be discussed here; further information can be found in the references cited below.

Extensive measurements on several types of fibre at high gamma-ray dose rates and neutron fluences have been reported and published [11-45, 11-46, 11-47, 11-48, 11-49] for commercially available monomode and multimode fibres. The results show that pure silica core fibres will be sufficiently radiation hard over the life time of the LHC operation, in contrast to Ge-doped core fibres. Specifically, measurements after gamma irradiation [11-48] lead to a predicted loss of 0.12 dB/year for an 8m long section of pure silica core monomode fibre in the inner detector region (10 kGy/year), while neutron irradiation of 100 m of 50 μm core pure silica multimode fibre [11-49] gives an attenuation of 0.8 dB after 2×10^{14} n/cm^2 of 1 MeV neutrons. Recovery due to subsequent annealing has not been included in these figures. This performance is completely adequate for binary readout, and radiation hard fibres are available from several manufacturers.

Radiation testing of MT-4 connectors has been carried out with 10 MRad of gammas and 2×10^{13}/cm^2 of neutrons [11-50] with no detectable degradation after 100 repeated connections and disconnections. Irradiation of MT-8 connectors (same design) with 10^{14} n/cm^2 is in progress [11-50].

Preliminary radiation testing of PIN-diodes mounted in the LED/PIN packages supplied by GEC-Marconi with 6×10^{13} p/cm^2 at the CERN PS indicate satisfactory performance [11-51]. Reirradiation of these devices with neutrons from a high-rate source[1] indicate significant damage at a fluence of 2×10^{14} n/cm^2. These results were obtained with the old-style PINs, where the rise time behaviour was in any case unacceptable. Further irradiations studies with the new epitaxial silicon PINs are being planned.

Irradiation studies of LEDs

The radiation hardness and life time of different optical emitters suitable for a fibre optic link for the SCT have been studied in detail since the submission of the technical proposal [11-52,11-53,11-54,11-55,11-56]. The scope of these studies has been twofold. The short term behaviour of LEDs during and shortly after irradiation was investigated by irradiating them under different operating conditions with neutron and proton fluences comparable to (and in some cases exceeding) those expected at LHC. After the irradiation, the diodes were subjected to an annealing treatment, which in most cases reduced the radiation damage considerably. In addition, the life time after irradiation was studied in an accelerated life time test, where a large number of devices were operated at elevated temperature for several months. In order to reach

1. The Dynamitron at the University of Birmingham, where the rates as high as 5×10^9 n/cm^2/s

the required statistics, a dedicated measurement system (the scanning machine), which allows for the long term operation and measurement of several hundred devices, was built.

The short term behaviour of irradiated LEDs is discussed here. A description of a corresponding study performed with VCSELs may be found in [11-56].

The degradation of LEDs due to irradiation is primarily a bulk damage effect which is caused by the displacement of atoms from their original lattice sites. The amount of such displacement damage can be measured by the non-ionising energy loss (NIEL) [11-57]. The primary effect of irradiation is to decrease the light output of LEDs at a fixed operating current.

In addition to the LEDs from GEC-Marconi, similar devices obtained from ABB Hafo were tested. For the radiation hardness and life time studies, about 170 ABB and about 180 GEC LEDs have been tested. While most of these LEDs were mounted without any further packaging on ceramic boards in order to allow their operation in the scanning machine, a number of LEDs of both types were purchased in the pig-tailed packages described above.

Most of the LEDs were irradiated once with either ~ 1 MeV neutrons at the RAL ISIS facility or the Birmingham Dynamitron, or with 24 GeV protons at the CERN PS, reaching fluences as high as 5×10^{14} n/cm^2 and 4×10^{14} p/cm^2, respectively. Further tests involving the re-irradiation of LEDs are in progress at the time of this writing. During the irradiation, some of the devices were operated with either pulsed or DC currents, while others were not biased. For practical reasons, most of the irradiation was done at ambient temperature, but a few GEC LEDs were irradiated at about -7˚C without observing any substantial difference in the resulting radiation damage. Using some of the pig-tailed LEDs, the light output was measured during the irradiation, but the majority of the measurements were made after bringing the devices from the radiation facility back to the laboratory. After the irradiation, most of the devices were operated under forward bias and were frequently measured for several days at different currents in order to study the annealing behaviour. Once the light output remained stable and no further annealing (or antiannealing) was observed, the devices were operated for several months at an elevated temperature in order to accelerate the aging and to study the life time after irradiation.

A typical behaviour of a LED that was not biased during the irradiation is shown in Figure 11-41: After irradiation with 4.4×10^{14} n/cm^2, the relative light output[1] of this particular GEC LED was decreased to a few percent. However, when the LED was operated after the irradiation at a forward current of 50 mA, a significant amount of annealing was observed, increasing the relative light output to ~50% within a few days.

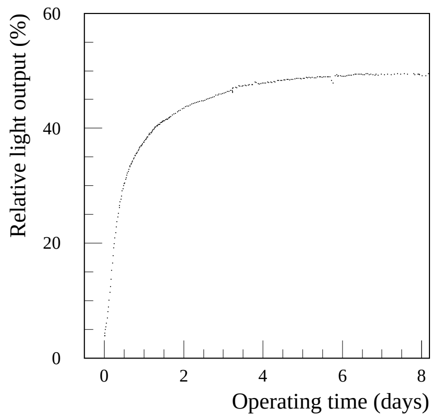

Figure 11-41 Relative light output of a GEC LED after irradiation with $4.4 \cdot 10^{14}$ n/cm^2 as a function of DC operating time at 50 mA and -10˚C.

Both the time needed for and the extent of the annealing after irradiation with a given fluence depend on the LED type and on the annealing current (most of the annealing studies were performed at either -10˚C or +10˚C). If

1. Since the linearity of LEDs changes slightly during irradiation and annealing, relative light outputs are always given for a nominal operating current of 10 mA (20 mA) for the ABB (GEC) LEDs, even though the annealing treatment may be done at a higher current.

the annealing current is too low, no or only very slow annealing is observed. While an increase of the annealing current often leads to more and faster annealing, it can also give rise to anti-annealing, thereby decreasing the light output with respect to the one reached at a lower annealing current. For the GEC LEDs, an annealing current of 50 mA was found to be sufficient up to fluences of about 4×10^{14} n/cm^2 and 2×10^{14} p/cm^2. Both annealing and anti-annealing have been observed after both proton and neutron irradiation.

If the LEDs are biased during the irradiation, as will be the case at LHC, depending on the radiation flux and the operating current, some or all of the annealing will take place during the irradiation. Consequently, the light output measured shortly after irradiation (i.e. before any additional annealing treatment is performed) is much higher than if the LEDs were off during the irradiation.

The results of the short term studies are summarized in Figure 11-42 by plotting the relative light output of individual LEDs after irradiation as a function of the fluence. The fluences for the neutron irradiation (with ~1MeV neutrons) at the RAL ISIS facility, and for the proton irradiation (with 24GeV protons) at the CERN PS, are given by the top and bottom axis, respectively. Using the NIEL calculations in [11-62] these axes were scaled such that the NIEL is the same for the corresponding neutron and proton fluences. Thus if the radiation damage in LEDs after the annealing can be parametrised by the NIEL, there should be no difference between neutron and proton irradiation data in Figure 11-42. Indeed, within the fairly large spread of the data, which may be partly due to uncertainties in the dosimetry, the proton and neutron irradiation results agree fairly well.

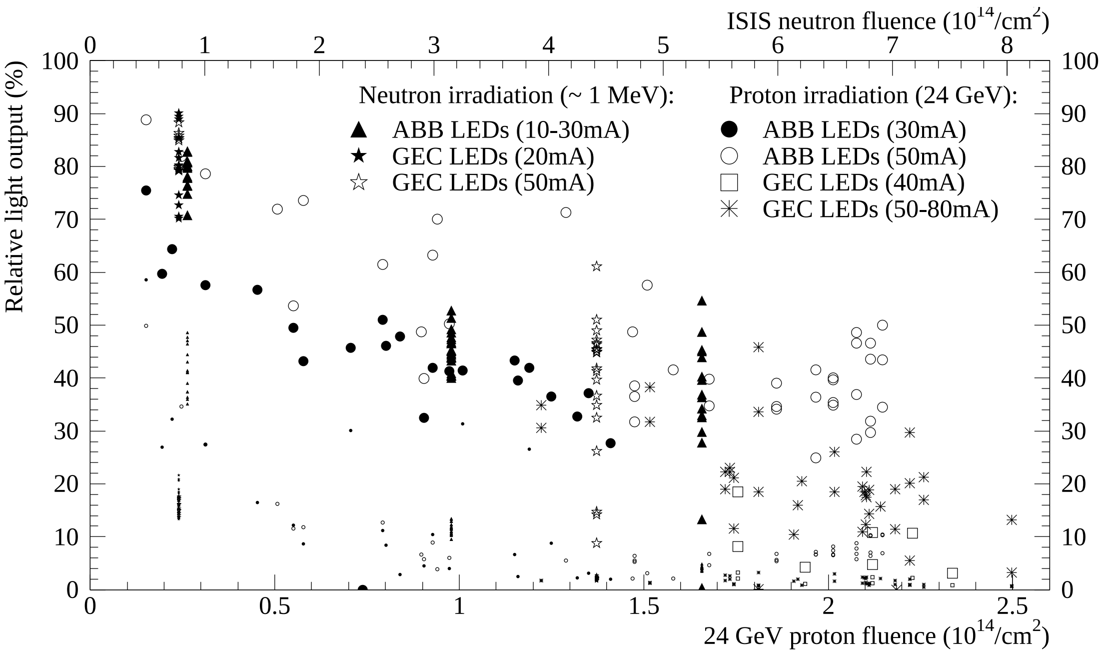

Figure 11-42 Relative light output of individual LEDs after irradiation as a function of fluence. The little dots denote the first measurement made after irradiation. The larger symbols show the relative light output after an annealing period of up to several weeks at the maximum forward current indicated in the legend. In most (but not all) cases, no signs of further annealing were observed. Both proton and neutron irradiation data is shown (see text).

The importance of injection annealing is evident from Figure 11-42 when comparing the measurements of the relative light output before (dots) and after (larger symbols) the annealing. The extent of the annealing observed at a given fluence depends on the maximum annealing current, as can be seen from a comparison of the ABB LEDs which were annealed at currents up to 30 mA (full circles) with those operated at currents up to 50 mA (hollow circles). It is also interesting to note that, after an adequate annealing period, no significant difference was found in the relative light output between LEDs that were biased with a DC or pulsed current during the irradiation (about one third of the LEDs) and LEDs that were off.

The distribution of the relative light output of GEC LEDs irradiated with 1.5 x 10^{14} to 2.5 x 10^{14} protons (24 GeV) per cm^2 after annealing at a maximum forward current between 50 mA and 80 mA is shown in Figure 11-43. Including proton and neutron irradiation data, 4 out of 59 GEC LEDs and 3 out of 91 ABB LEDs gave less than 10% of the initial light output after irradiation and subsequent annealing.

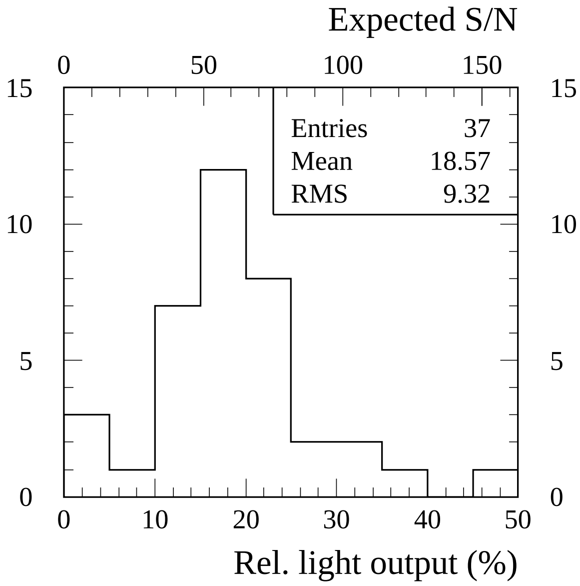

Figure 11-43 Distribution of relative light output of GEC LEDs irradiated with between 1.5 x 10^{14} and 2.5 x 10^{14} 24 GeV protons/cm^2 after annealing at a maximum forward current between 50 mA and 80 mA. The scale at the top of the figure shows the corresponding S/N for optical links after 10 years of operation, based on the estimate given in Table 11-17. Note that the resulting S/N distribution does not take into account the distribution of the initial light output of the LEDs.

11.4.6.4 Reliability

The components of the data transmission system within the detector volume will not be accessible once the detector is closed. It is therefore important to study the reliability of the system and of the components. One aspect of reliability has already been discussed, namely the redundancy scheme for clock and command transmission. A study of the life time of the LEDs and estimates of the signal to noise available after the degradation of the LEDs due to irradiation are now discussed.

Life time tests of LEDs

While it is well known that the light output of LEDs may be decreased after irradiation, little information seems to be available about the influence of radiation on the aging properties and thus on the life time of LEDs. In order to study this issue the irradiated LEDs were operated for several months once the annealing was completed. As for most life time tests, the aging had to be accelerated in order to obtain results within a reasonable time. Since aging of LEDs takes place only under forward bias, an acceleration factor of 12 is achieved with respect to the operation at LHC already by operating the LEDs in DC mode. This acceleration factor is based on the estimate that *i)* over 10 years, LHC will be running about one third of the time, *ii)* the average link occupancy should not exceed 50% to avoid loss of data, *iii)* the number of 0 and 1 bits is balanced in the data, and *iv)* the LEDs are switched off when no data is transmitted. The aging of LEDs can also be accelerated by increasing the operating temperature or current. The dependence of the mean LED life time τ on the junction temperature T and the forward current I is given by

$$\tau = C \cdot I^{-n} \cdot \exp\frac{E_a}{kT} \tag{11-5}$$

where the constants C, n and the thermal activation energy E_a depend on the composition and the fabrication process of the LED and must be determined experimentally for each type of LED. Values found in the literature for n and E_a are typically in the range from 1 to 2, and from 0.4eV to 1.0eV, respectively.

For most of the life time studies, an operating temperature of 50˚C and a nominal operating current of 10mA (20mA) for the ABB (GEC) LEDs were chosen. Because E_a is not known for both the ABB and the GEC LEDs, the additional acceleration factor for the operation at 50˚C cannot be calculated with precision. However, if a nominal operating temperature of 10˚C is assumed (the LED operating temperature in the SCT is expected to be between about -10˚C and +10˚C), the typical values of E_a found in the literature result in acceleration factors from 8 to 160 for the operation at 50˚C. Therefore, as a conservative estimate, an additional acceleration factor of 10 is assumed for the aging at 50˚C.

Table 11-16 Summary of the statistics and the operating time achieved in the LED life time studies. The numbers quoted are the current statistics available at the time of writing. Final numbers will be presented in [11-56].

LED Type	Part.	Fluences ($10^{14}/cm^2$)	Irrad. LEDs	DC operating time at ±10˚C / 50˚C (days)	Corresponding time in the SCT (years)
ABB pigtailed	n	1.4 ± 20%	5	162 / 158	57
ABB pigtailed	n	1.4 ± 20%	5	272 / 0	9
ABB unpackaged	n	3.2 / 5.3	39	1..35 / 123..126	~41
ABB unpackaged	p	0.6 .. 2.2	52	6 .. 44 / 59 .. 126	20 .. 43
GEC unpackaged	n	4.4	12	15 .. 18 / 39	~13
GEC unpackaged	p	1.2 .. 2.5	31	18 .. 40 / 39 .. 106	13 .. 36

The results of the life time studies are summarized in Table 11-16, which shows the operating time achieved during the annealing (at 10˚C) and during the life time studies (at 50˚C) for different groups of LEDs irradiated with different particles and fluences. LEDs which were damaged mechanically (e.g. broken bonding wires) or which had an initial light output below 5µW coupled into a multimode fibre before the irradiation are not included in these statistics. The last column gives an estimate of the corresponding operating time in the SCT. This estimate takes into account an acceleration factor of 12 due to DC operation and, for the operation at 50˚C, an additional factor of 10 as discussed above. Acceleration of the aging due to elevated currents applied during the annealing treatment is not taken into account. No devices failed during the high temperature operation.

Results with a prototype link

Measurements have been made on a prototype LED - fibre - PIN diode optical link. The LED and optical fibre proposed for the ATLAS system were used. A very fast silicon PIN diode[1] and a low noise trans-impedance amplifier designed for opto-electronic receivers comprised the receiver [11-61]. A commercial discriminator[2] was used after the amplifier. The speed of the receiver amplifier can be adjusted by altering the current in the feedback loop. As the speed of the amplifier is increased, the noise-bandwidth of the amplifier is increased hence total noise increases. If the bandwidth is too low there will be a loss of signal amplitude. Therefore for a given data transmission speed there is an optimal amplifier speed. The results of such an optimisation are shown in Figure 11-44. where the signal to noise ratio is shown as a function of the amplifier 10-90% rise time, with the link being used to send NRZ data at 40 Mbits/s.

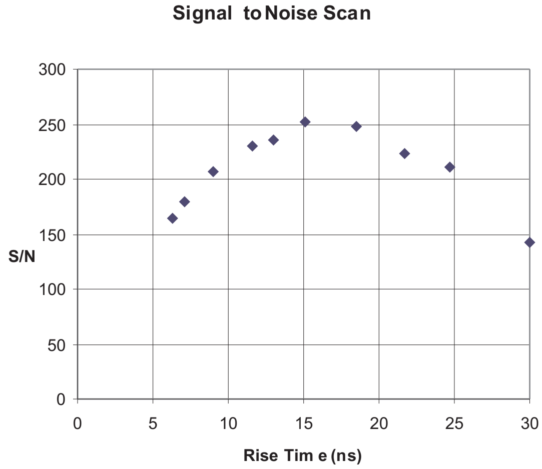

Figure 11-44 Amplifier Optimisation.

A signal to noise ratio of 250 was achieved with this prototype. Some changes in S/N are anticipated for the ATLAS system, and a S/N calculation relevant to operation after 10 years at LHC is given in Table 11-17. This table allows one to translate the information on relative light output obtained from the irradiation studies to S/N. The scale at the top of Figure 11-43 shows the expected distribution of S/N for links using components irradiated at fluences greater than or equal to those expected in the SCT. For a link to operate at a bit error rate of less than 10^{-9} the S/N must be greater than 12.4 although allowing for the standard engineering safety factors would require a S/N greater than 20. Provided that the LEDs with higher than average initial light output are used at the innermost layers, then even for fluences beyond the maximum expected, the links have a reasonable margin of safety.

11.4.6.5 Material budget

The routing of the optical fibres follows that of the power cables. The material budget of the fibres, including protective coating, is estimated to be at most 5% of the corresponding power cable material. The contribution from the LED/PIN package is approximately 0.005% X_0 per SCT module at $\theta = 90^0$.

1. Honeywell HFD3013
2. Philips NE5224

Table 11-17 Estimated average S/N of optical links after 10 years of operation.

S/N measured with prototype	**250**
Correct for operating temperature	1.20
Prototype LED power/average LED power	1.09
Higher responsivity PINs	1.5
Lower PIN noise due to shorter leads	1.1
Attenuation in 2 MT connectors	0.83
Attenuation in 88m fibre	0.9
Possible atten. due to rad-hard to standard fibre coupling	0.9
Expected S/N before irradiation	363
LED degradation after irradiation with 2 x 10^{14} pcm^{-2}	0.2
Attenuation due to fibre irradiation	0.9
Estimated average S/N after 10 years operation	65

11.4.6.6 Future developments

In the ATLAS application the occupancy of the link will vary from near zero during Cosmic Ray data taking to close to 100% during high luminosity running. Hence a simple AC coupled scheme for the amplifier - discriminator connection as used in the prototype link would not work. However it would be very difficult to make the amplifier stable for a pure DC coupled scheme to work. A DC coupled scheme with regular compensation for the amplifier offset drift is proposed. The scheme is illustrated inFigure 11-45. The transimpedance amplifier and discriminator would be integrated into one IC and the temperature stability of the amplifier would be optimised.

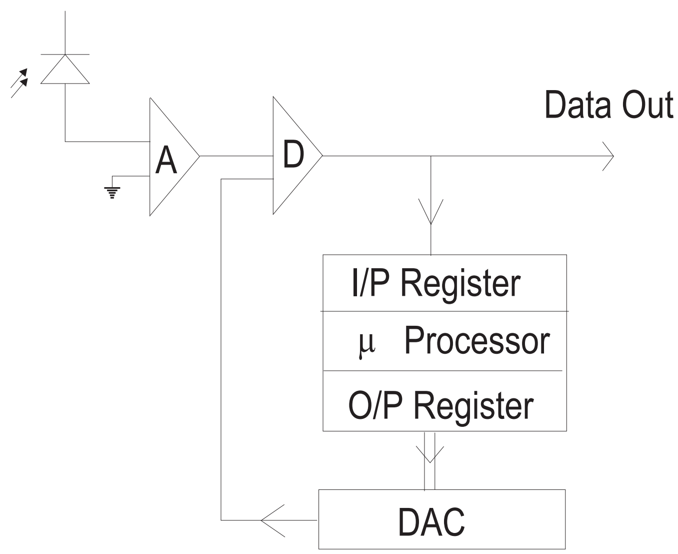

Figure 11-45 Principle of compensated DC coupled scheme. A is a linear amplifier and D is a discriminator.

At regular intervals (i.e. of the order of every hour) the following calibration sequences would be performed:

- No Signal calibration. With no data being sent the micro Processor would adjust the DAC values until ones were detected by the input register. The DAC value at which there was a 50% probability to record a one, V_{low} would be recorded.
- Signal Calibration. With a string of alternate zeros and ones being sent the micro Processor would adjust the DAC values until there was a 50% probability of recording a one as a one. This DAC value, V_{high} would be recorded.
- DAC setting. The optimal setting of the threshold so as to minimise the BER is to set it half way between the no signal and signal levels. Hence the optimal value for the DAC setting would be V_{DAC}= 0.5(V_{low}+V_{high}).

The system can also be used to monitor the noise of the link by measuring the width of the threshold curves. Hence the system could use the knowledge of the signal amplitudes and noise to provide error reporting.

11.4.7 Cables

11.4.7.1 Cable requirements and design

In addition to the job of supplying power, there are two main important concerns in the power distribution system. These are the grounding, which is discussed in Section 11.4.9, and mass minimisation. The maximum voltage drop for a given voltage rail, and the maximum power dissipation in the corresponding cable, determine the material introduced by cables. In the case of SCT this is important for the two high-current low-voltage lines (see Section 11.4.8) as all others can be as thin as technologically possible. The maximum voltage drop for these two critical lines is chosen such that if the current draw were to drop to zero, the maximum voltage which would appear on any chip in the system would not exceed its specification. The power dissipation this yields is acceptable.

Low mass cables (tapes) are used to supply low-voltage (4.0V and 3.5V) to on-module electronics, high voltage for detector bias, PIN diode bias, temperature and low voltage sensing as well as various signals for module functions. There is one low mass tape per module. Its cross section is shown in Figure 11-46. Table 11-18 summarises the tape's properties. The tape is made from two single sided flat cables with a 25 µm thick Kapton coverlayer over the exposed conductor surface. The sandwich is bonded using PU glue. The cables are fabricated from an aluminium-Kapton laminate[1]. The tape run is divided into an inner part from the modules to a patch panel at the cryostat wall and an outer part from this patch panel to the patch panel close to the muon system. From the second patch panel, the cabling continues with conventional cables. The maximum signal length in low mass tape is 6 m, the longest single piece is 4.2 m. The aluminium thickness is 50 µm for the inner and 100 µm for the outer part. The Kapton substrate thickness is 50 µm. The lines on the cable have a minimum width and separation of 0.5 mm and are produced by a lithographic procedure. The cable ends are electochemically nickel plated to prevent oxidation of the contacts. The connection to the module pigtail / patch panel is made by clamping cable ends into two zero insertion-force connectors (ELCO ZIF Series 6200) on each end.

1. (prod. no. PN 60420AL), supplied by GTS Materiaux flexibles SARL, F-91968 Les Ulis

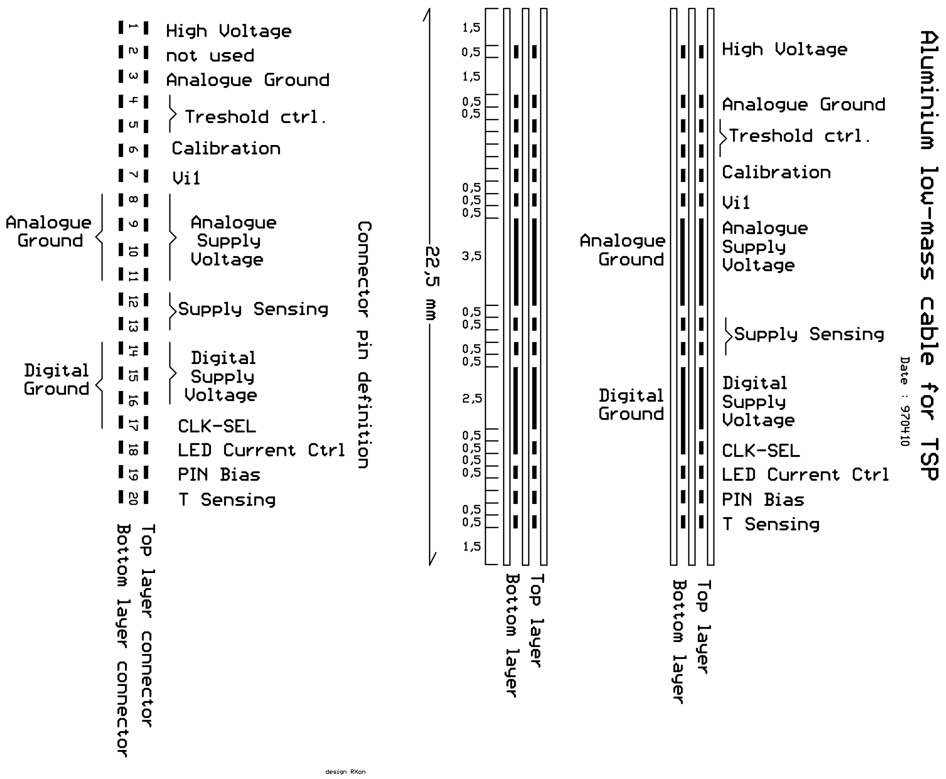

Figure 11-46 Cross section through a low mass power tape, inside the detector volume.

The cable design takes into account heat dissipation, geometric constraints and permissible voltage drops. Aluminium was selected as the conductor because it has four times the conductivity of copper per radiation length. The aluminium is thicker in the outer part where material is not as critical. The largest voltage drop is ~0.5 V yielding a total heat production of ~3 kW, of which < 1 kW is in the cold volume of the SCT.

11.4.7.2 Material budget

Table 11-19 shows the material contribution associated with the cables. Reduction of the aluminium below 50 μm is ineffective as the Kapton then becomes the dominant material contribution.

11.4.7.3 Radiation hardness

Radiation hardness of kapton has been tested by the manufacturer and shows no degradation for dose levels up to 100KGy and a volume resistance drops by only a factor of 3 even at a dose of 10 MGy. This change (which corresponds to a much higher dose than expected) would cause only insignificant change (~10 nA) in the detector bias current. Rupture and mechanical strength, elastic modulus and dielectric constant remained almost unaffected. Glues were tested by the CERN-TIS group and they find no significant degradation of epoxy glues for doses up to 1 MGy.

Table 11-18 Low mass cable parameters.

overall cable width	22.5 mm
cable run	3-6 meter
cable thickness	~250 or 350 μm
50 μm Al cross section	1.45 mm^2
100 μm Al cross section	2.90 mm^2
Kapton cross section	3.53 mm^2
Aluminium resistivity	0.028 ohm mm^2 /meter
Voltage drop on 3.5 V line in the barrel	0.55 (±0.08) volt
Voltage drop on 3.5 V line in the forward	0.56 (+0.11,-0.24) volt
Voltage drop on 4.0 V line in the barrel	0.39 (± 0.06) volt
Voltage drop on 4.0 V line in forward	0.40 (+0.08, -0.17) volt
Barrel cables power inside at -10 C	250 watt
Forward cables power inside at -10 C	655 watt
Total inside power at -10 C	905 watt
Barrel cables power to cryostat	545 watt
Forward cables power to cryostat	925 watt
Total power to cryostat patch panel	1500 watt
Barrel power cryostat to muon patch panel	880 watt
Forward power cryostat to muon patch panel	400 watt
Total second part	1300 watt
Total power in low mass cables	2800 watt

Table 11-19 Cable material contributions

aluminium radiation length	89 mm
Kapton radiation length	350 mm
single connector averaged over module	0.07 % X_0
single cable	0.11 % X_0
single cable averaged over module	0.04 % X_0
end of stave averages over module (6 cables)	0.26 % X_0
barrel cables (1056) at r=520 mm	0.85 % X_0
barrel cables (1056) at r=1150 mm (cryostat)	0.38 % X_0
forward cables (988) at r=620 mm	0.67 % X_0
all cables in crack (r=1200 mm) (100 μm Al)	1.16 % X_0

11.4.8 Power Supplies

11.4.8.1 Overview

The SCT modules are powered with a set of low voltages (LV) for front-end electronics and a high voltage (HV) for detector bias. The power supply system also provides a set of control lines to the module. The voltages are:

- +3.5 V analog power for bipolar amplifier/discriminator circuits,
- +4.0 V digital power for CMOS pipeline circuits, DORIC3, a front-end clock and L1 distribution chip, and a dual LED driver circuit LDC,
- +10 V PIN photo-diode voltage for a diode connected to DORIC input,
- detector bias voltage, and
- low current control lines.

The power supply system has current, voltage and temperature monitoring features as well as overcurrent protection and safety systems.

11.4.8.2 Modularity and specification

The modularity of SCT power supplies follow the modularity of the detector so that 4088 power supplies serve the 2112 barrel and 1976 forward detector modules.

The required parameter values for the LV and HV power from each supply are summarised in Table 11-20. In addition to voltages listed, a bipolar preamplifier current control is required. The maximum current of this voltage is 6 mA per module (0.5 mA per chip).

Table 11-20 Required parameters for the SCT power supplies.

Parameter	Analogue Voltage	Digital Voltage	PIN Voltage	Bias Voltage
Nominal value [V]	3.50 ± 5%	4.00 ± 5%	10.00±5%	10 - 300
Maximum current	900 mA	240 mA	10 μA	4 μA - 4 mA
Voltage setting resolution [V]	0.01	0.01	0.1	1.0
Current monitoring accuracy	1 mA	1 mA	1 μA	multirange
Time for voltage adjustment	100 μs	100 μs	100 μs	20 ms
Start/stop ramping	unspecified	>2 V/s	unspecified	unspecified
Over-current trip at	1200 mA	350 mA	12μA	programmable
Over-voltage trip at	5.50 V	6.00 V	11.00V	400 V
Allowable ripple (peak to peak)	35 mV	35 mV	100 mV	200 mV

11.4.8.3 Design of the SCT low voltage supply

LV separated power supplies for six detector modules are mounted on a standard 6U card and are mounted in a EUROcrate. One crate can contain up to 20 cards served by an SAB80C517A crate controller. An interface with other crate controllers as well as with an external computer will be realized in CAN-bus standard.

The crates are supplied with 50 V DC (obtained from 380 V AC). A DC to DC converter on each power channel operates at a frequency of 100 kHz. All the voltages are separately adjustable. Monitoring of currents, output voltages and temperatures is performed on the card. Channel ON/OFF functions and over-current protection are also integrated into the functionality of each 6U board. A schematic block diagram of an LV crate and one power channel is shown in Figure 11-47.

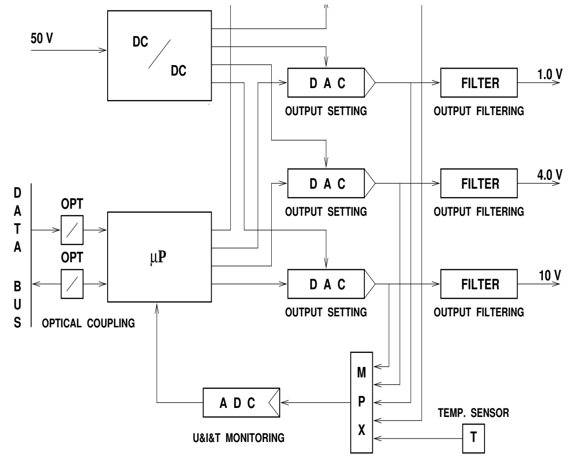

Figure 11-47 Block Diagram of LV Power Module and Crate.

11.4.8.4 Design of the SCT high voltage supply

The HV power supply modules are also mounted on 6U cards in EUROcrates. In this case, each card has 12 channels together with their control circuits.

Each HV channel is supplied from a separate secondary winding of a 50Hz transformer, which ensures DC isolation. A simplified diagram of the HV power card is shown in Figure 11-48.

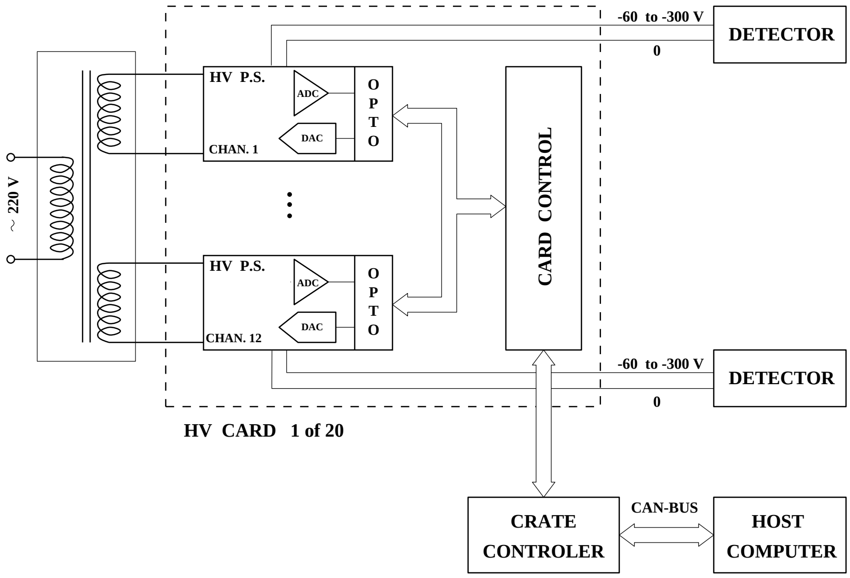

Figure 11-48 Block Diagram of HV Power Card.

The required voltage value is set and monitored using DACs and ADCs. Current monitoring with sufficient precision and dynamic range requires a two-step operational amplifier circuit. The overcurrent circuit can reduce the current and voltage to values to close to zero. Every channel has its own separated supply for monitoring circuits and channel control and digital output of measurements are transmitted via opto-couplers to help control grounding.

11.4.8.5 Supply location and power distribution

Two possible locations are still under evaluation for the power supply location. These are: in the USA15 cavern outside the tunnel; and on shelves on the outer shell of the ATLAS detector.

In the latter case the power supply modules are closer to detector modules by about 60 meters on average, but they must operate in a 200-400 gauss magnetic field. It is expected that an access is possible during short 1-day shutdowns of the machine. The primary motivation of this location is the price of the conventional power cables running to the first patch panel.

In either location, the low voltage and bias voltage power supply modules serving the same detector module will be close together. A patch panel will allow grouping of all lines belonging to a detector module in one multi-wire cable.

11.4.9 Grounding

Controlling pickup and cross-coupling has been a formidable challenge in all existing silicon vertex detectors. The ATLAS SCT is ~50 times larger in scale than any existing vertex detector. More important, unlike existing collider vertex detectors, data readout will proceed concurrently with the acquisition of low-level signals from the strip sensors. Since the binary readout system, like all on-chip sparsification schemes, requires local (i.e. on-detector) signal threshold discrimination, the system must be designed to minimize and, equally important, to control the introduction of spurious signals into the front-end amplifiers.

The SCT has adopted a “groundless” system, because

- in a large-scale system designed for minimum mass there is no low- impedance, equipotential common ground,
- common grounds cross-couple disparate parts of the system and often introduce interference,
- signal transfer from the silicon sensor to the electronics and between electronics stages *does not require a ground*; instead, it is essential to provide well-controlled signal current return paths that are not shared with potential interference sources,
- spurious grounds can only be controlled by requiring that systems be designed ungrounded, and ground connections should only be made deliberately where they are shown to be necessary.

The general grounding policy for ATLAS and the Inner Detector are described in Section 13.3, and the related safety aspects are covered in Section 16.5.

The detector is electrically compartmentalised by utilising separate power supply channels and power tapes for each module. Individual voltage sources are referenced to ground and one another through high-value resistors. Use of individual supplies per module also allows the direct

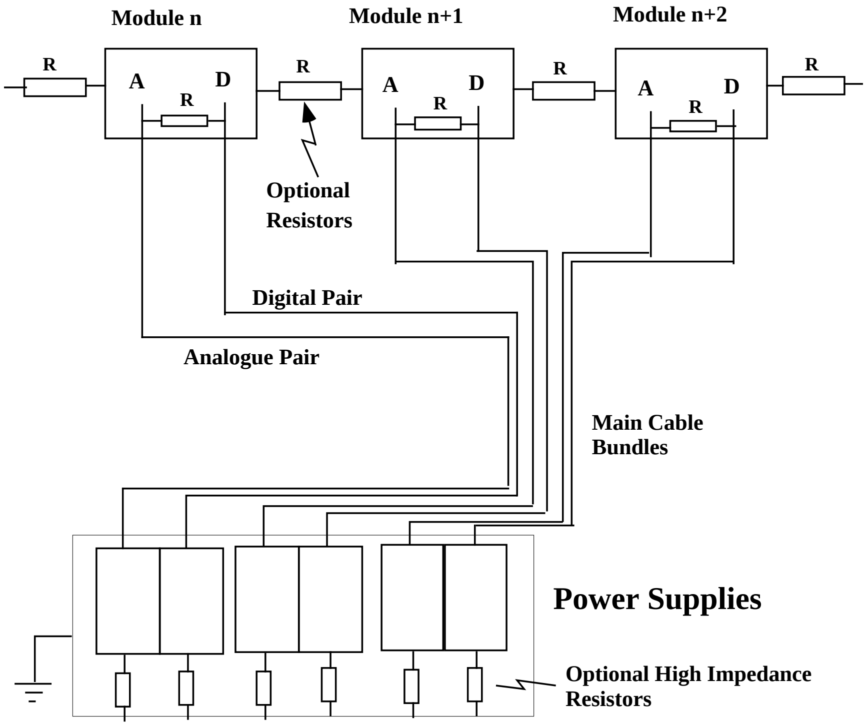

Figure 11-49 Grounding Arrangement.

monitoring of module currents and reduces the circuitry (material) on the module. The basic arrangement is shown in Figure 11-49.

It is obvious that for signal integrity, spurious AC coupling paths are a matter of concern. Capacitive or inductive coupling can form ground returns even in the absence of a DC ground connection. This problem must be addressed by proper electronic and module design, as will be discussed below.

One advantage of the readout architecture adopted by the ATLAS SCT is that analog signals are confined to the module and that within a module, analog activity does not go beyond the first stages on the front-end IC. This eliminates corruption of analog signals on the readout busses or links. Furthermore, the front-end circuitry has been designed to reduce signal sensitivity through both power supply connections (i.e. V_{CC} and “Gnd”).

The critical requirement is to reduce the introduction of interference into the input of the front-end. The most susceptible path is through the detector backplane. The second critical path is the signal current loop comprising the detector and the connection to the input transistor. This loop includes the neighbour strips and, to a lesser degree, the backplane of the detector. The backplane connection is most susceptible, as it involves a bus that connects the emitters of all input transistors on one face of a module and for practical reasons cannot provide the most direct connection. Good filtering of any connections to this node is critical, in addition to avoiding any connections to “grounds” that could introduce spurious signals.

Introduction of interference into the input signal path has two primary origins:

- coupling through the backplane of the detector,
- readout (digital) current spikes propagating towards the front-end.

The second path has been essentially blocked by incorporating special interface circuitry between the analog and digital portions of the front-end ICs to present a high impedance to signals originating in the digital circuitry [11-64]. This also allows separation of both analog and digital power supply busses (including "ground"). It also facilitates local isolation between the common input bus and the remainder of the circuitry. It should be noted that this arrangement also decouples the front-end from cross-coupling through the power tapes and allows isolation of the front-end circuitry from spurious AC "grounds" on the readout lines. Implementation of this scheme is simplified in a two-chip scheme as implemented in CAFE-M + ABC. In a single chip readout such as ABCD, the same type of circuitry can be used, but cross-coupling through the substrate must be avoided. The DMILL SOI technology used in ABCD may by itself provide sufficient isolation. If necessary, the substrate can be electrically "partitioned" as in the ATOM chip designed for the BaBar experiment[11-65]. The first path, coupling into the backplane of the detector, can be formed by pickup to the detector bias lines, by bypass capacitors that introduce interference from "ground" or by coupling from the mechanical mount. All of these interference paths are exacerbated by common grounds. In the SCT all voltage supplies are treated as differential lines, with dedicated pairs of lines for positive and negative ("ground") connections of the single voltage analog and digital supplies and the detector bias voltage. The detector bias voltage will be filtered in both legs of the balanced line. The current design of the baseline module also provides a low-capacitance (< 1 pF) mount to the support structure to reduce direct coupling to the backplane through that path.

The redundancy scheme requires that adjacent modules be connected to transfer the clock. This connection will be through appropriately designed differential links to preserve isolation. The necessary DC referencing will be provided by high-value resistors.

To control cross-coupling between the SCT and the TRT, a thin cylindrical Faraday shield will surround the SCT. The penetrations for the cables and services distributed around the circumference of the detector render hermetic shielding impractical, but coverage will be sufficient to provide significant isolation between the SCT and TRT. This shield will be connected to the shields surrounding the cable bundles emanating from the outer layer and disk modules.

The basic arrangement described above has been used in several test beam runs at CERN and KEK since 1994. As many as six binary modules at a time have been operated with 40 MHz readout clocks in a parallel mounting arrangement that tends to increase coupling between modules relative to the edge-to-edge overlap in the SCT. The modules were electrically isolated and the readout cables bundled parallel over a 20m run to the counting area. Six modules also form a barrel local support, so this configuration approximates a representative module set with respect to the cross-coupling of bundled power tapes. Consistently, noise levels measured in the beam position are the same as measured for individual modules in the lab. No special noise optimization was required. A similar design philosophy was followed in the design of the CDF silicon vertex detector, which has used on-chip sparsification successfully in routine operation since 1992 [11-66].

Clearly, although encouraging, these results are not sufficient to verify the design. More work on larger scale assemblies is required and is planned for 1997 and 1998. Nevertheless, an important feature of this arrangement is that it provides the ability to control ground connections and monitor them, while retaining the flexibility to implement modifications, should the need arise.

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