11 The Semiconductor Tracker

11.1 Introduction

11.1.1 Introductory Discussion

The Semiconductor Tracker (SCT) is a sub-detector of the ATLAS Inner Detector (ID). The SCT works with the other elements of the ID, the Transistion Radiation Tracker (TRT) and the Pixel Tracker to provide the necessary tracking functions to meet the performance requirements discussed in the Inner Detector Perormance Section (Chapter 2). The SCT is based upon silicon microstrip detector technology. This approach has been used with success over the past 8 years in experiments at LEP [11-1] and at the Fermilab Tevatron [11-2]. Consequently there is substantial experience in the high energy physics community with the construction and operation of these devices.

The challenges posed by the ATLAS SCT are primarily those of radiation damage and scale. In the case of radiation damage, these devices are expected to experience fluences ~10^{34} $cm^{-2}s^{-1}$, 10-20 times higher than in past applications. This has led to a substantial development effort aimed at ensuring adequate radiation resistance in the design, and this is discussed in detail in this document. The SCT has an active silicon area of ~$63m^2$, more than 50 times that of any existing silicon vertex detector. In addition, precision mechanical and cooling techniques, used successfully in the vertex detectors, must be engineered on a cylindrical scale of diameter 1m and length 6m, a factor 10 larger than before. These challenges and their solutions will be discussed in detail in this document. Because of the difficulties posed by the LHC operating environment and requirements of reliability, a technically conservative design for the SCT tracker has been developed. Where possible, safety factors and redundancy have been implemented in the design. The design optimisation has been carried out within the conflicting requirements of low cost and stringent limits on radiation and absorption length.

11.1.2 Purpose and Scope of the SCT TDR

The purpose of this document is to describe the design of the Semiconductor Tracker and to describe how the device will be constructed, assembled, and installed in ATLAS. In this document each SCT design consideration will be placed within the context of constraints imposed by performance specifications and by the LHC operating environment.

The design of the SCT is based upon an extensive R&D program. It is not possible to review the entire program, nor to discuss in detail the technical alternatives considered en route. The detail given in this design report varies. Critical areas such as the silicon detectors and the frontend electronics are fully described and documented in sufficient detail to allow the technical viability of the project to be judged and for construction to begin. Items such as the support structure and services are not on the critical path and are still being optimised.

11.1.3 Organisation of the SCT TDR

The Semiconductor Tracker TDR chapter is organized into 13 sections including this Introduction. The sections are organized as described below.

Global Issues

In Section 11.2, we describe the overall SCT design and the issues which motivate its global design and operation. In the Introduction, we summarize the issues and specifications which effect the design and present the basic layout. This is followed by a detailed description of the layout and geometry in Section 11.2.2. In Section 11.2.3, we decribe the LHC operational conditions and the impact of these conditions on the overall tracker design. In particular the expected radiation fluences and their uncertainties are presented. Finally, in Section 11.2.4, the motivation for the most important technology and system choices of the ATLAS SCT, is placed in context with the layout and operating environment.

Technical Design

The detailed technical design of the SCT is described in Section 11.3 through Section 11.8, which cover in order the detector design, the electronics and readout, the module design, calibration and monitoring, the cooling, and the support structure. In each section we initially present a discussion of the effect of the LHC and ATLAS operating environment on the element. We then present a specification for the element, a detailed technical description of the design, the expected and simulated performance where relevant, and relevant prototype results in support of the design choice. Finally, a detailed compilation of the material in the detector and associated services is presented in Section 11.9.

Construction and Assembly

Section 11.10 and Section 11.11 describe the SCT construction and assembly procedure. The construction process is necessarily hierarchical; elements such as front end ICs and silicon sensors are the basic blocks from which the system is constructed. Consequently the discussion is organized into a sub-section on module construction, a sub-section on the assembly of modules onto supports, supports into barrels and disks, then interlinks, and enclosures. At the level of module construction, activity will take place across the geographic span of the SCT community and involve aspects ranging from component testing and qualification, to the electrical and mechanical testing of complete modules. A discussion of principles adopted by the SCT to facilitate this process will be given.

Prototyping and System Tests

In Section 11.12, ongoing and planned activities aimed at further prototyping and testing of the baseline elements of the SCT are described. These activities are either aimed at technical optimisations within the baselines or at understanding issues of the electrical and mechanical interaction of sub-units of the SCT. A discussion is given of planned work on detectors, front end electronics, modules, and mechanics. We then describe two major system tests, the TSP (Tracker Sector Prototype) for the 1998 test beam, and a planned system test of a full forward disk assembly.

Project Organisation and Management

In Section 11.13, organisational and management issues are described. An overview is given, in terms of the SCT itself and also as an element of the Inner Detector. A list of participating institutes and authors is presented. The organisation of the SCT community into various working groups is described, together with a matrix of tasks and responsibilities. Schedules and milestones are presented, and finally a description of the project costs and resources is given.

11.1.4 References

11-1 B. Mours et al., The Design, Construction and Performance of the ALEPH Silicon Vertex Detector, Nucl. Instr. Methods A379 (1996), 101-115.
V. Chabaud et al., The DELPHI Silicon Strip Microvertex Detector with Double Sided Readout, Nucl. Instr. Methods A368 (1996), 314-332.
M. Acciarri et al., The L3 Silicon Microvertex Detector, Nucl. Instr. Methods A360 (1995), 103-109.
P. Allport et al., The OPAL Silicon Strip Microvertex Detector with Two Coordinate Readout, Nucl. Instr. methods A346 (1994), 476-495.

11-2 J. Antos et al., The SVX-II Silicon vertex Detector Upgrade at CDF, Nucl. Instr. methods A360 (1995), 118-124, and references therein.